MICROCHIP

AT27C256R

256-Kbit (32K x 8) One-Time Programmable, Read-Only Memory

Features

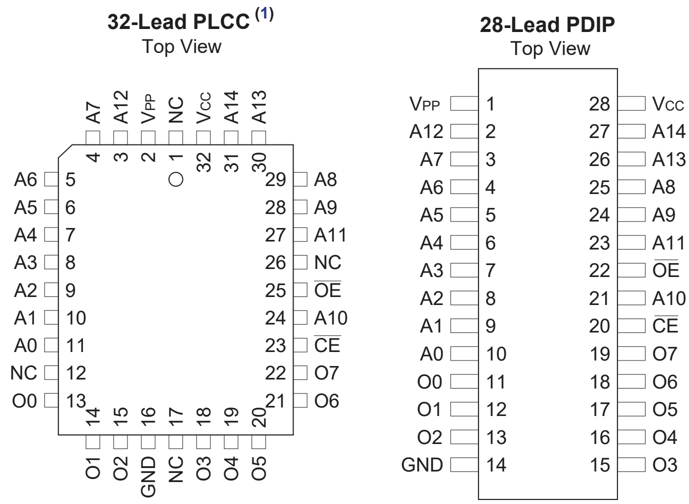
- Fast Read Access Time: 45 ns
- Low-Power CMOS Operation:
  - 100 µA Maximum standby
  - 20 mA Maximum active at 5 MHz
- 5V ± 10% Supply
- High Reliability CMOS Technology:
  - 2,000V ESD protection
  - 200 mA Latch-up immunity
- Rapid Programming Algorithm – 100 µs/byte (typical)
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Industrial Temperature Range: -40°C to +85°C
- Green Package Options (Lead-free/Halide-free/RoHS compliant)

Packages

- 32-Lead PLCC and 28-Lead PDIP

Table of Contents

1. Package Types (not to scale)



Note:

1. PLCC package pins 1 and 17 are “don’t connect”.

2. Pin Description

The description of the pins are listed in Table 2.1.

Table 2-1. Pin Description

Name	32-Lead PLCC	28-Lead PDIP	Function
A0 - A14	3-11; 24; 27-31	2-10; 21; 23-27	Address inputs
O0 - O7	13-15; 18-22	11-13; 15-19	Outputs
$\overline{CE}$	23	20	Chip Enable
$\overline{OE}$	25	22	Output Enable
NC	1; 12; 17; 26	—	No Connect
V_{PP}	2	1	Programming Voltage
V_{CC}	32	28	Device Power Supply
GND	16	14	Ground

3. Description

The Microchip AT27C256R is a low-power, high-performance, 262,144-bit, One-Time Programmable, Read-Only memory (OTP EPROM) organized as 32,768 words of 8 bits each. It requires only one 5V power supply in normal Read mode operation. Any byte can be accessed in less than 45 ns, eliminating the need for speed reducing WAIT states on high-performance microprocessor systems.

The Microchip scaled CMOS technology provides low active power consumption and fast programming. Power consumption is typically only 8 mA in active mode and less than 10 μA in Standby mode.

The AT27C256R is available in a choice of industry-standard, JEDEC-approved, PDIP and PLCC packages. All devices feature two-line control (CE, OE) to give designers the flexibility to prevent bus contention.

With 32 Kbyte storage capability, the AT27C256R allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

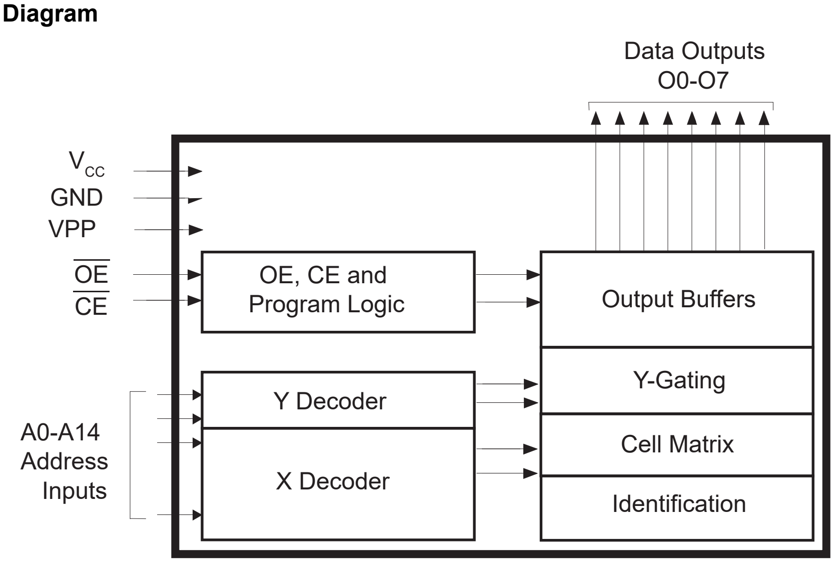
The AT27C256R has additional features to ensure high quality and efficient production use. The rapid programming algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 μs/byte. The integrated product identification code electronically identifies the device and manufacturer. This feature is used by industry-standard programming equipment to select the proper programming algorithms and voltages.

3.1 System Considerations

Switching between active and standby conditions via the chip enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed datasheet limits, resulting in device non-conformance. At a minimum, a 0.1 μF, high-frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 μF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

3.2 Block Diagram

Figure 3-1. Block Diagram



4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Temperature under bias	-55°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on any pin with respect to ground	-2.0V to +7.0V(1)
Voltage on A9 with respect to ground	-2.0V to +14.0V(1)
V_{PP} supply voltage with respect to ground	-2.0V to +14.0V(1)

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:

1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} +0.75V DC, which may overshoot to +7.0V for pulses of less than 20 ns.

4.2 DC and AC Operating Range

Table 4-1. DC and AC Operating Range

Mode/Pin	$\overline{CE}$	$\overline{OE}$	Ai	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	Ai	V_{CC}	D_{OUT}
Output disable	V_{IL}	V_{IH}	X(1)	V_{CC}	High-Z
Standby	V_{IH}	X(1)	X(1)	V_{CC}	High-Z
Rapid program(2)	V_{IL}	V_{IH}	Ai	V_{PP}	D_{IN}
PGM verify(2)	X(1)	V_{IL}	Ai	V_{PP}	D_{OUT}
Optional PGM verify (2)	V_{IL}	V_{IL}	Ai	V_{CC}	D_{OUT}
PGM inhibit(2)	V_{IH}	V_{IH}	X(1)	V_{PP}	High-Z
Product identification(4)	V_{IL}	V_{IL}	A9 = V_H(3) A0 = V_{IH} or V_{IL} A1-A14 = V_{IL}	V_{CC}	Identification code

Notes:

1. X can be V_{IL} or V_{IH}.
2. Refer to programming characteristics.
3. $V_H = 12.0 \pm 0.5V$.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9, which is set to V_H, and A0, which is toggled low (V_{IL}) to select the manufacturer's identification byte and high (V_{IH}) to select the device code byte.

Table 4-2. DC and AC Operating Conditions for Read Operation

AT27C256R		-45	-70
Operating Temperature (Case)	Industrial Temperature Range	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%

4.3 DC and Operating Characteristics for Read Operation

Table 4-3. DC and Operating Characteristics for Read Operation

Parameter	Symbol	Minimum	Maximum	Units	Condition	
Input Load Current	I_{LI}	—	±1	µA	Industrial	V_{IN} = 0V to V_{CC}
Output Leakage Current	I_{LO}	—	±5	µA	Industrial	V_{OUT} = 0V to V_{CC}
V_{PP}[1] Read/Standby Current	I_{PP1}[2]	—	10	µA	V_{PP} = V_{CC}	
V_{CC}[1]Standby Current	I_{SB}	—	100	µA	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ±0.3V	
			1	mA	I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} +0.5V	
V_{CC} Active Current	I_{CC}	—	20	mA	f = 5 MHz, I_{OUT} = 0 mA, $\overline{E}$ = V_{IL}	
Input Low Voltage	V_{IL}	-0.6	0.8	V		
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.5	V		
Output Low Voltage	V_{OL}	—	0.4	V	I_{OL} = 2.1 mA	
Output High Voltage	V_{OH}	2.4	—	—	I_{OH} = -400 µA	

Notes:
1. V_{CC} must be applied simultaneously with or before V_{PP}, and removed simultaneously with or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

4.4 AC Characteristics for Read Operation

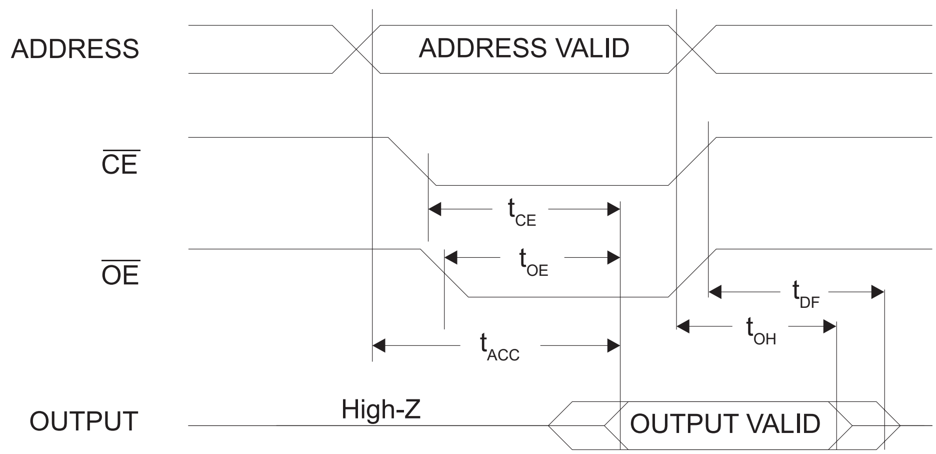
Table 4-4. AC Characteristics for Read Operation

Parameter	Symbol	-45		-70		Units	Condition
		Minimum	Maximum	Minimum	Maximum		
Address to Output Delay	t_{ACC}[1]	—	45	—	70	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}[1]	—	45	—	70	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}[1]	—	20	—	30	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ or $\overline{CE}$ High to Output Float, Whichever Occurred First	t_{DF}[1]	—	20	—	25	ns	$\overline{OE}$ or $\overline{CE}$ High to Output Float, Whichever Occurred First

...........continued							
Parameter	Symbol	-45		-70		Units	Condition
		Minimum	Maximum	Minimum	Maximum		
Output hold from address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	t_{OH}	7	—	7	—	ns	Output hold from address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first

Note:
1. See Figure 4-1.

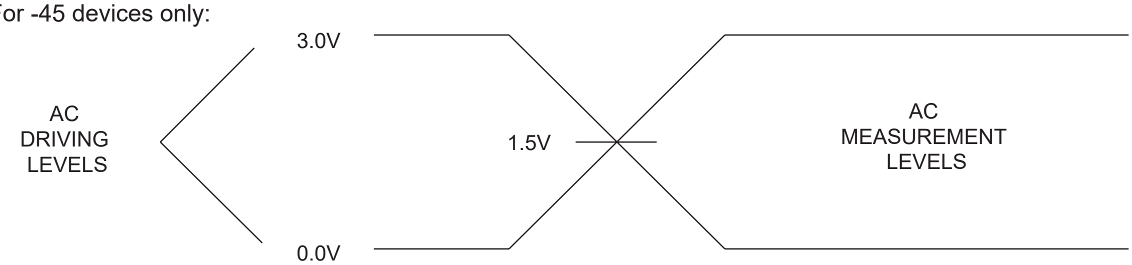
Figure 4-1. AC Waveform for Read Operation



Notes:
1. Timing measurement reference level is 1.5V for -45 devices. Input AC drive levels are V_{IL} = 0.0V and V_{IH} = 3.0V. Timing measurement reference levels for all other speed grades are V_{OL} = 0.8V and V_{OH} = 2.0V. Input AC drive levels are V_{IL} = 0.45V and V_{IH} = 2.4V.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled, and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

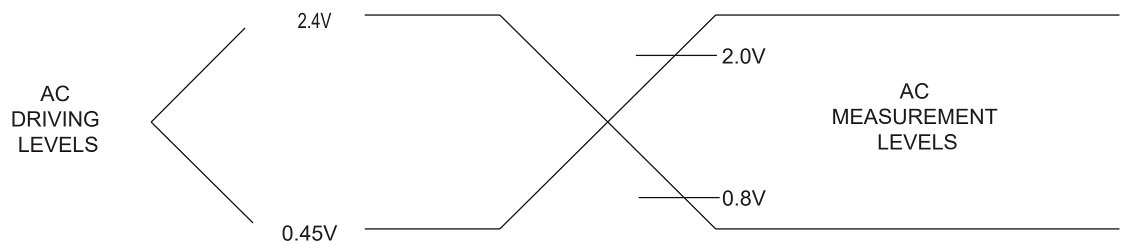
Figure 4-2. Input Test Waveforms and Measurement Levels

For -45 devices only:



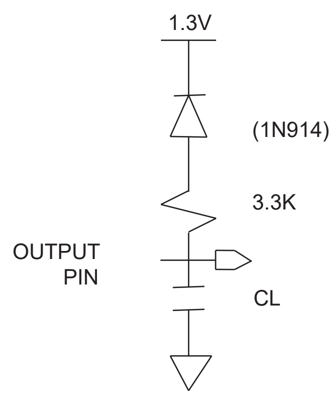
t_R, t_F < 5 ns (10% to 90%)

For -70 devices:



t_R, t_F < 20 ns (10% to 90%)

Figure 4-3. Output Test Load

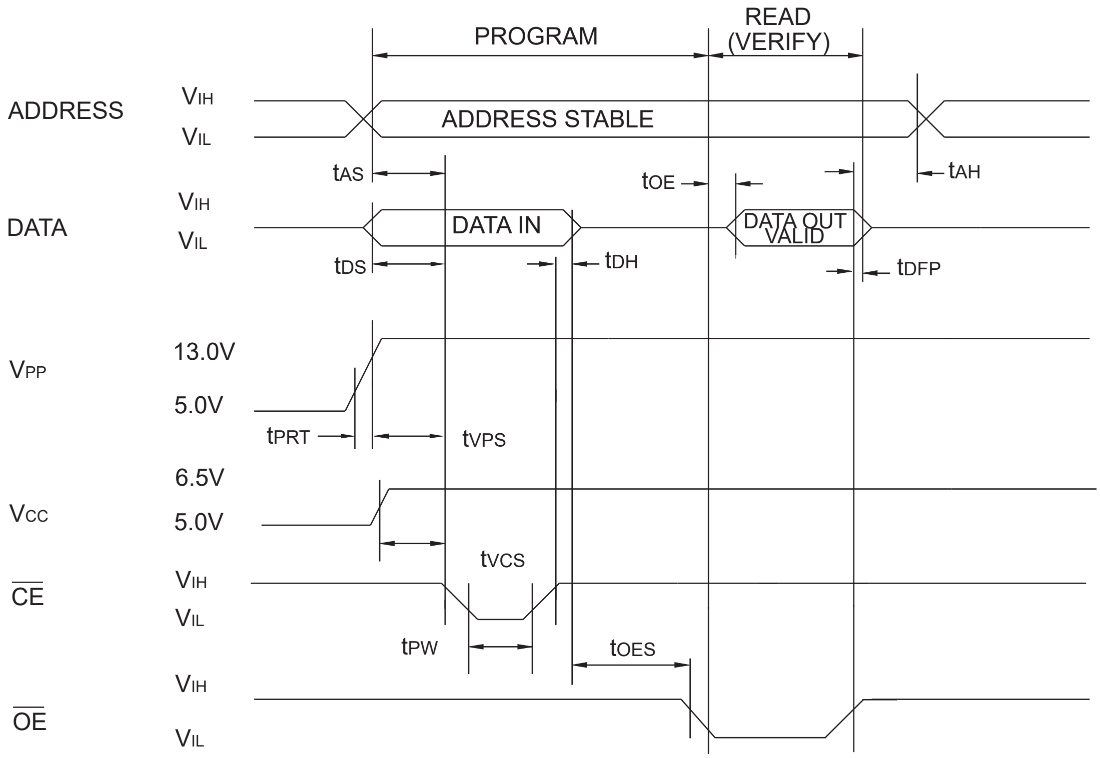


Note:

1. CL = 100 pF including jig capacitance, except for the -45 devices, where CL = 30 pF.

4.5 Programming Waveforms

Figure 4-4. Programming Waveforms



Notes:

1. The input timing reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device, but must be accommodated by the programmer.
3. When programming the AT27C256R, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

4.6 DC Programming Characteristics

Table 4-5. DC Programming Characteristics [(1)]

Parameter	Symbol	Limits		Units	Test Conditions
		Minimum	Maximum		
Input Load Current	I_{LI}	—	±10	µA	$V_{IN} = V_{IL}, V_{IH}$
Input Low Level	V_{IL}	-0.6	0.8	V	
Input High Level	V_{IH}	2.0	V_{CC} + 1	V	
Output Low Voltage	V_{OL}	—	0.4	V	I_{OL} = 2.1 mA
Output High Voltage	V_{OH}	2.4	—	V	I_{OH} = -400 µA
V_{CC} Supply Current (Program and Verify)	I_{CC2}	—	25	mA	
V_{PP} Current	I_{PP2}	—	25	mA	$\overline{CE} = V_{IL}$

...........continued

Parameter	Symbol	Limits		Units	Test Conditions
		Minimum	Maximum		
A9 Product Identification Voltage	V_{ID}	11.5	12.5	V	

Note:

1. T_A = +25 ± 5°C, V_{CC}= 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

4.7 AC Programming Characteristics

Table 4-6. AC Programming Characteristics

Parameter	Symbol	Limits		Units	Test conditions
		Minimum	Maximum		
Address Setup Time	t_{AS}	2	—	µs	Input rise and fall times (10% to 90%) 20 ns Input pulse levels 0.45V to 2.4V Input timing reference level 0.8V to 2.0V Output timing reference level 0.8V to 2.0V
$\overline{OE}$ Setup Time	t_{OES}	2	—	µs	
Data Setup Time	t_{DS}	2	—	µs	
Address Hold Time	t_{AH}	0	—	µs	
Data Hold Time	t_{DH}	2	—	µs	
$\overline{OE}$ High to Output Float Delay(2)	t_{DFP}	0	130	ns	
V_{PP} Setup Time	t_{VPS}	2	—	µs	
V_{CC} Setup Time	t_{VCS}	2	—	µs	
$\overline{CE}$ Program Pulse Width(3)	t_{PW}	95	105	µs	
Data Valid From $\overline{OE}$(2)	t_{OE}	—	150	ns	
V_{PP} Pulse Rise Time During Programming	t_{PRT}	50	—	ns	

Notes:

1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}.
2. This parameter is only sampled, and is not 100% tested. Output float is defined as the point where data is no longer driven. See timing diagram.
3. Program pulse width tolerance is 100 µs ± 5%.

4.8 Electrical Specifications

4.8.1 Pin Capacitance

Table 4-7. Pin Capacitance(1,2)

Symbol	Typical	Maximum	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes:
1. This parameter is characterized but is not 100% tested in production.
2. f = 1 MHz, T_A = 25°C

4.9 Integrated Product Identification Code

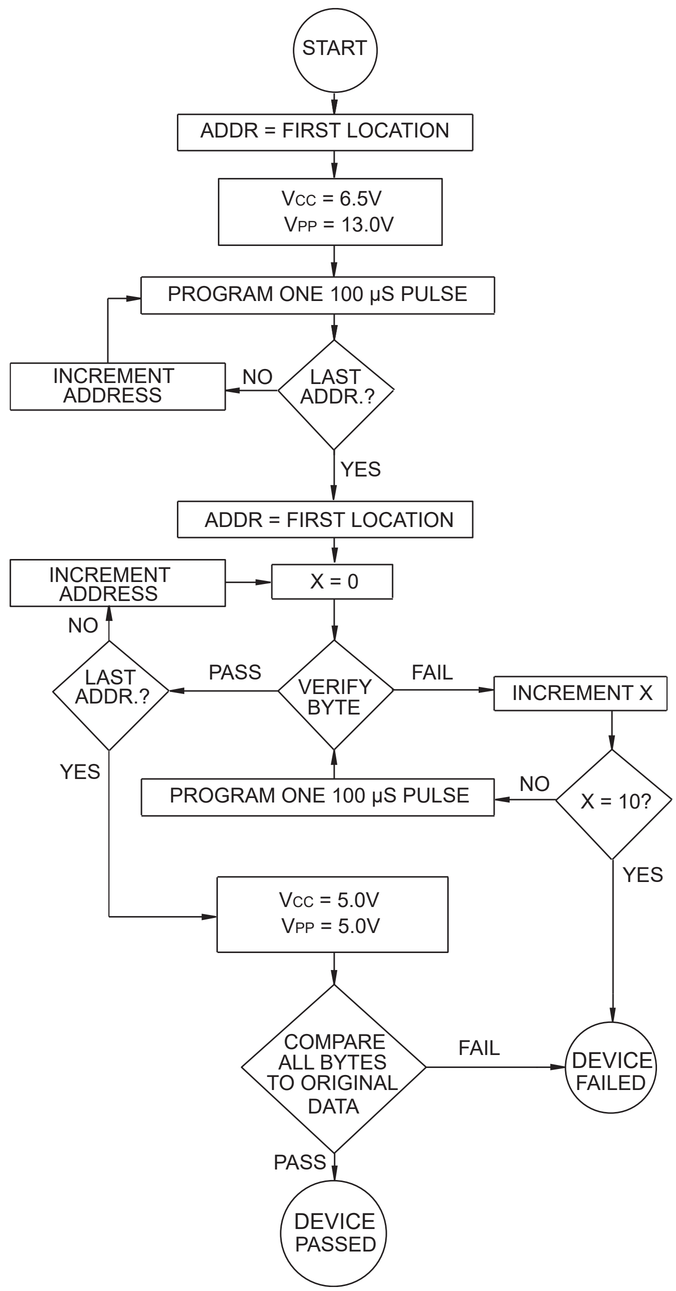
Table 4-8. Integrated Product Identification Code

Codes	Pins									Hex data
	A0	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device type	1	1	0	0	0	1	1	0	0	8C

5. Rapid Programming Algorithm

A 100 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100 µs $\overline{CE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.

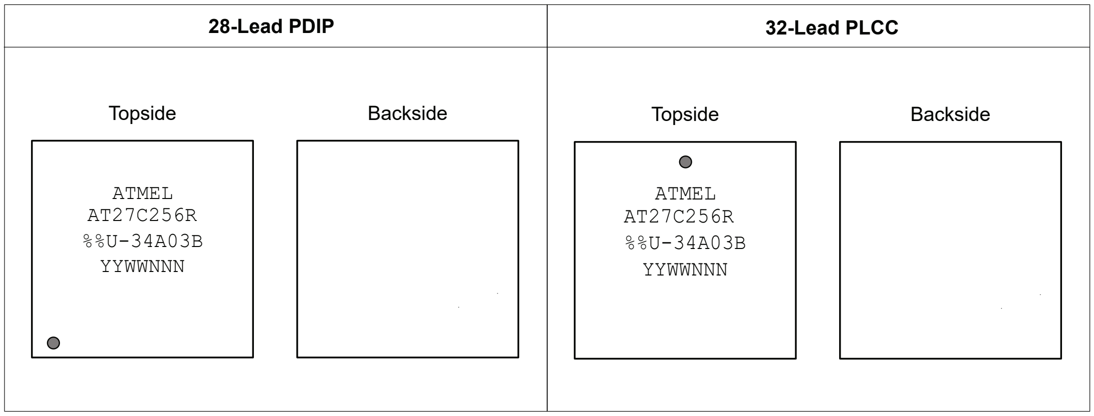
Figure 5-1. Rapid Programming Algorithm



6. Packaging Information

6.1 Package Marking Information

AT27C256R: Package Marking Information

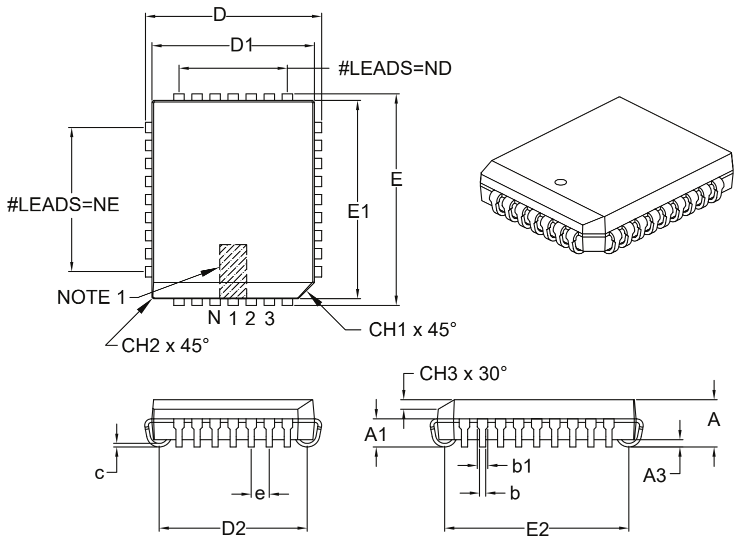


Note: no backside markings

		%% = Access Time	
		45: 45 ns 70: 70 ns	
		Lot Trace Code	
		YWWNNN: Lot Trace Code Y: Year, WW: Work Week NNN = Assembly Trace Code	

32-Lead Plastic Leaded Chip Carrier (L) – Rectangle [PLCC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



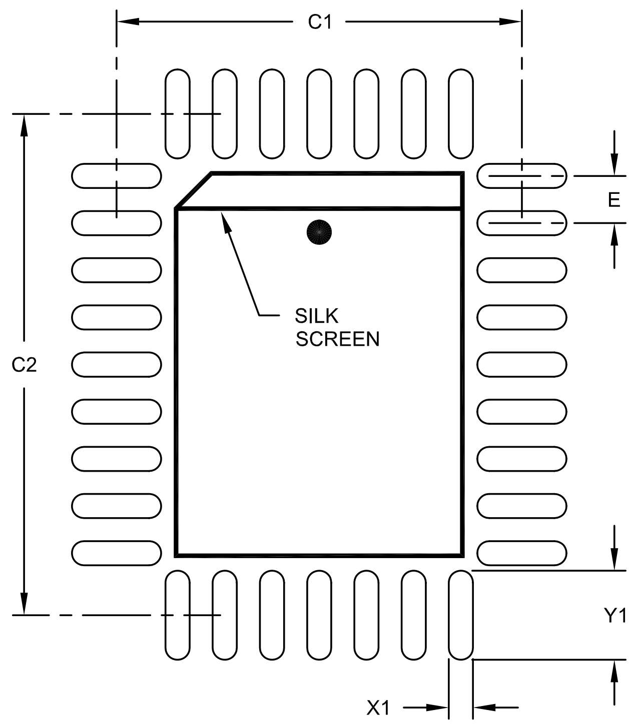
Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	32		
Pitch	e	.050		
Pins along Length	ND	7		
Pins along Width	NE	9		
Overall Height	A	.125	–	.140
Contact Height	A1	.060	–	.095
Standoff §	A3	.015	–	–
Corner Chamfer	CH1	.042	–	.048
Chamfers	CH2	–	–	.020
Side Chamfer Height	CH3	.023	–	.029
Overall Length	D	.485	–	.495
Overall Width	E	.585	–	.595
Molded Package Length	D1	.447	–	.453
Molded Package Width	E1	.547	–	.553
Footprint Length	D2	.376	–	.446
Footprint Width	E2	.476	–	.546
Lead Thickness	c	.008	–	.013
Upper Lead Width	b1	.026	–	.032
Lower Lead Width	b	.013	–	.021

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

Microchip Technology Drawing C04-023B

32-Lead Plastic Leaded Chip Carrier (L) - Rectangle [PLCC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		.050 BSC	
Contact Pad Spacing	C1		.429	
Contact Pad Spacing	C2		.531	
Contact Pad Width (X32)	X1			,026
Contact Pad Length (X32)	Y1			.094

Notes:

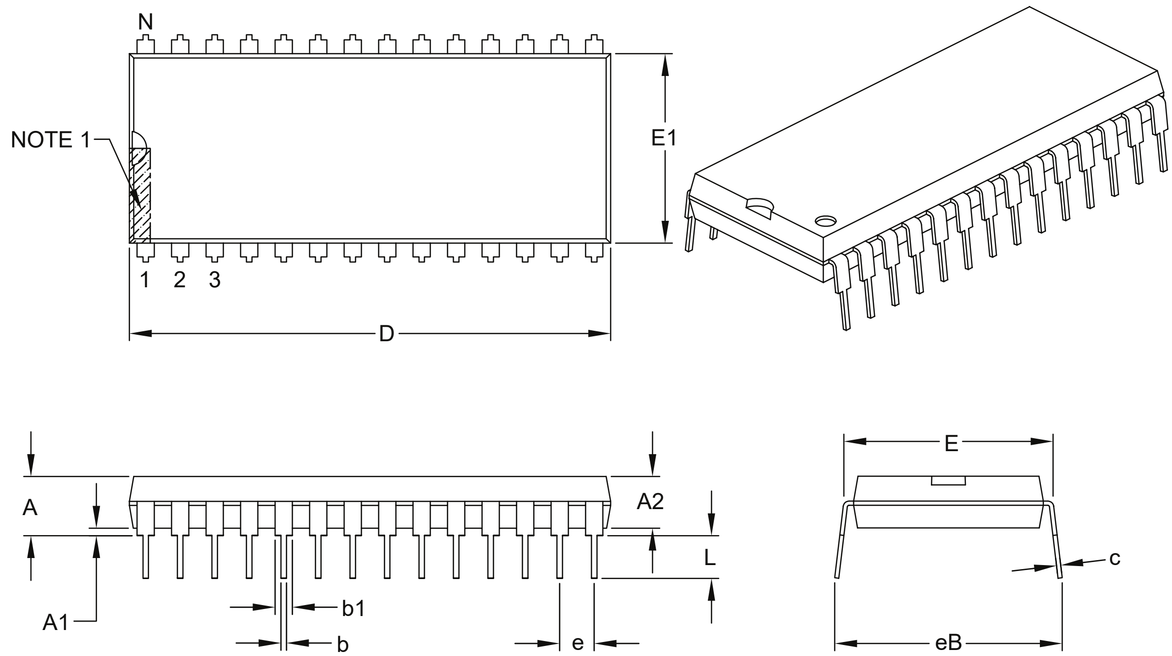
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2023A

28-Lead Plastic Dual In-Line (P) – 600 mil Body [PDIP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.250
Molded Package Thickness	A2	.125	–	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.590	–	.625
Molded Package Width	E1	.485	–	.580
Overall Length	D	1.380	–	1.565
Tip to Seating Plane	L	.115	–	.200
Lead Thickness	c	.008	–	.015
Upper Lead Width	b1	.030	–	.070
Lower Lead Width	b	.014	–	.022
Overall Row Spacing §	eB	–	–	.700

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-079B

7. Revision History

Revision A (May 2022)
Updated to the Microchip template. Microchip DS20006674 replaces Atmel document 0014. Updated Part Marking Information. Updated section content throughout for clarification. Updated the PLCC and PDIP package drawings to the Microchip equivalents.

Atmel Document 0014 Revision O (October 2011)
Correct pinouts.

Atmel Document 0014 Revision N (April 2011)
Remove TSOP and SOIC packages; Add lead finish to ordering information.

Atmel Document 0014 Revision M (December 2007)

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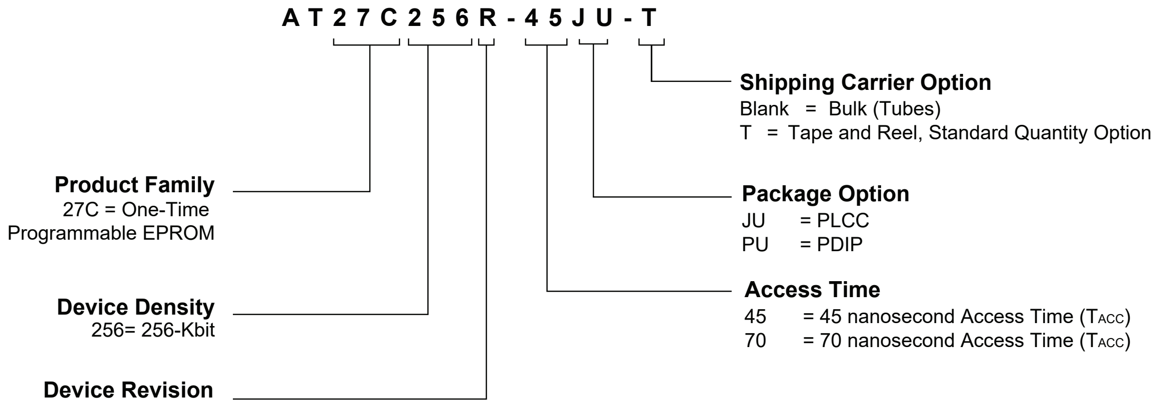
Product Identification System

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Examples

Device	Package	Package Drawing Code	Package Option	Shipping Carrier Option	Device Grade
AT27C256R-45JU	PLCC	L	JU	Bulk (Tubes)	Industrial Temperature (-40°C to +85°C)
AT27C256R-70JU	PLCC	L	JU	Bulk (Tubes)	
AT27C256R-45PU	PDIP	P	PU	Bulk (Tubes)	
AT27C256R-70PU	PDIP	P	PU	Bulk (Tubes)	
AT27C256R-45JU-T	PLCC	L	JU	Tape and Reel	
AT27C256R-70JU-T	PLCC	L	JU	Tape and Reel	

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