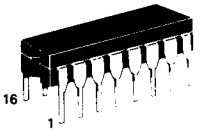
# MC6875
# MC6875A

## M6800 TWO-PHASE CLOCK GENERATOR/DRIVER

SCHOTTKY MONOLITHIC INTEGRATED CIRCUIT




L SUFFIX
CERAMIC PACKAGE
CASE 620

## M6800 CLOCK GENERATOR

Intended to supply the non-overlapping $\phi 1$ and $\phi 2$ clock signals required by the microprocessor, this clock generator is compatible with 1.0, 1.5, and 2.0 MHz versions of the MC6800. Both the oscillator and high capacitance driver elements are included along with numerous other logic accessory functions for easy system expansion.

Schottky technology is employed for high speed and PNP-buffered inputs are employed for NMOS compatibility. A single +5 V power supply, and a crystal or RC network for frequency determination are required.

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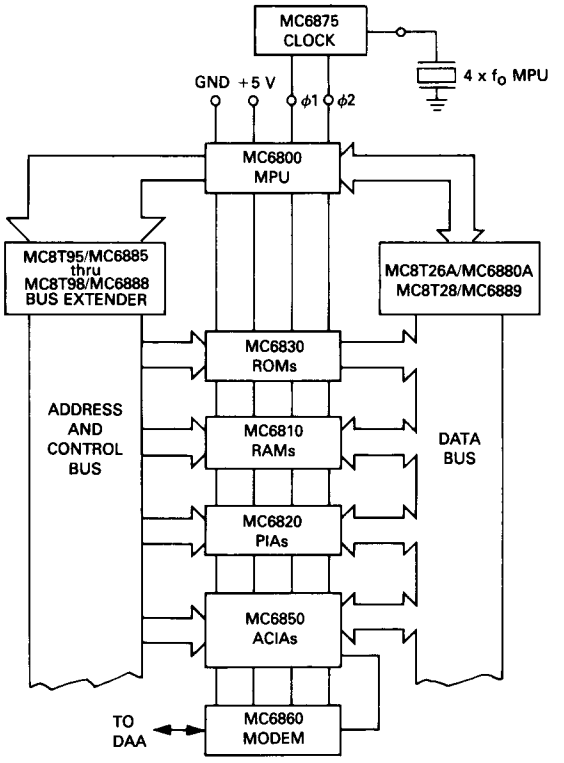
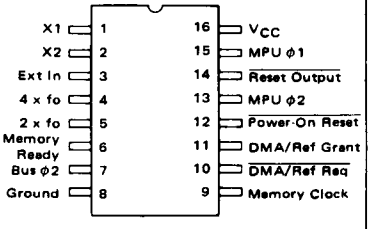
Typical MPU System with Bus Extenders




PIN CONNECTIONS




ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| MC6875L | 0 to +70°C | Ceramic DIP |
| MC6875AL | −55 to +125°C | |

**MAXIMUM RATINGS** (Unless otherwise noted $T_A$ = 25°C.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | +7.0 | Vdc |
| Input Voltage | $V_I$ | +5.5 | Vdc |
| Operating Ambient Temperature Range<br>MC6875L<br>MC6875AL | $T_A$ | <br>0 to +70<br>-55 to +125 | °C |
| Storage Temperature Range | $T_{stg}$ | -65 to +150 | °C |
| Operating Junction Temperature | $T_J$ | 175 | °C |

NOTE:
Operation of the MC6875AL over the full military temperature range (to maximum $T_A$) will result in excessive operating junction temperature.

The use of a clip on 16 pin heat sink similar to AAVID Engineering, Inc., Model 5007 ($R_{\theta CA}$ = 18°C/W) is recommended above $T_A$ ≈ 95°C.

Contact AAVID Engineering, Inc.
30 Cook Court
Laconia, New Hampshire 03246
Tel. (603) 524-4443

**RECOMMENDED OPERATING CONDITIONS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | +4.75 to +5.25 | Vdc |

**ELECTRICAL CHARACTERISTICS**
(Unless otherwise noted specifications apply over recommended power supply and temperature ranges.
Typical values measured at $V_{CC}$ = 5.0 V and $T_A$ = 25°C.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage — High Logic State | | | | | |
| MPU $\phi$1 and $\phi$2 Outputs | | | | | V |
| ($V_{CC}$ = 4.75 V, $I_{OHM}$ = -200 μA) | $V_{OHM}$ | $V_{CC}$ - 0.6 | – | – | |
| ($V_{CC}$ = 5.25 V, $I_{OHMK}$ = +5.0 mA) | $V_{OHMK}$ | – | – | $V_{CC}$ + 1.0 | |
| Bus $\phi$2 Output | | | | | V |
| ($V_{CC}$ = 4.75 V, $I_{OHB}$ = -10 mA) | $V_{OHB}$ | 2.4 | – | – | |
| ($V_{CC}$ = 5.25 V, $I_{OHBK}$ = +5.0 mA) | $V_{OHBK}$ | – | – | $V_{CC}$ + 1.0 | |
| 4 x fo Output | | | | | V |
| ($V_{CC}$ = 4.75 V, $V_{IH}$ = 2.0 V, $I_{OH4X}$ = -500 μA) | $V_{OH4X}$ | 2.4 | – | – | |
| 2 x fo, DMA/Refresh Grant and Memory Clock Outputs | | | | | V |
| ($V_{CC}$ = 4.75 V, $I_{OH}$ = -500 μA) | $V_{OH}$ | 2.4 | – | – | |
| $\overline{\text{Reset}}$ Output | | | | | V |
| ($V_{CC}$ = 4.75 V, $V_{IH}$ = 3.3 V, $I_{OH\overline{R}}$ = -100 μA) | $V_{OH\overline{R}}$ | 2.4 | – | – | |
| Output Voltage — Low Logic State | | | | | |
| MPU $\phi$1 and $\phi$2 Outputs | | | | | V |
| ($V_{CC}$ = 4.75 V, $I_{OLM}$ = +200 μA) | $V_{OLM}$ | – | – | 0.4 | |
| ($V_{CC}$ = 4.75 V, $I_{OLMK}$ = -5.0 mA) | $V_{OLMK}$ | – | – | -1.0 | |
| Bus $\phi$2 Output | | | | | V |
| ($V_{CC}$ = 4.75 V, $I_{OLB}$ = +48 mA) | $V_{OLB}$ | – | – | 0.5 | |
| ($V_{CC}$ = 4.75 V, $I_{OLBK}$ = -5.0 mA) | $V_{OLBK}$ | – | – | -1.0 | |
| 4 x fo Output | | | | | V |
| ($V_{CC}$ = 4.75 V, $V_{IL}$ = 0.8 V, $I_{OL4X}$ = 16 mA) | $V_{OL4X}$ | – | – | 0.5 | |
| 2 x fo, DMA/Refresh Grant and Memory Clock Outputs | | | | | V |
| ($V_{CC}$ = 4.75 V, $I_{OL}$ = 16 mA) | $V_{OL}$ | – | – | 0.5 | |
| $\overline{\text{Reset}}$ Output | | | | | V |
| ($V_{CC}$ = 4.75 V, $V_{IL}$ = 0.8 V, $I_{OL\overline{R}}$ = 3.2 mA) | $V_{OL\overline{R}}$ | – | – | 0.5 | |
| Input Voltage — High Logic State | | | | | V |
| Ext. In, Memory Ready and $\overline{\text{DMA/Refresh Request}}$ Inputs | $V_{IH}$ | 2.0 | – | – | |
| Input Voltage — Low Logic State | | | | | V |
| Ext. In, Memory Ready and $\overline{\text{DMA/Refresh Request}}$ Inputs | $V_{IL}$ | – | – | 0.8 | |
| Input Thresholds — $\overline{\text{Power-On Reset}}$ Input (See Figure 2) | | | | | V |
| Output Low to High | $V_{ILH}$ | – | 2.8 | 3.6 | |
| Output High to Low | $V_{IHL}$ | 0.8 | 1.4 | – | |
| Input Clamp Voltage MC6875L | $V_{IK}$ | – | – | -1.0 | V |
| ($V_{CC}$ = 4.75 V, $I_{IC}$ = -5.0 mA) MC6875AL | | – | – | -1.5 | |
| Input Current — High Logic State | | | | | |
| Ext. In, Memory Ready and $\overline{\text{DMA/Refresh Request}}$ Inputs | $I_{IH}$ | – | – | 25 | μA |
| ($V_{CC}$ = 4.75 V, $V_{IH}$ = 5.0 V) | | | | | |
| $\overline{\text{Power-On Reset}}$ | $I_{IH\overline{R}}$ | – | – | 50 | μA |
| ($V_{CC}$ = 5.0 V, $V_{IH\overline{R}}$ = 5.0 V) | | | | | |
| Input Current — Low Logic State | | | | | |
| Ext. In, Memory Ready and $\overline{\text{DMA/Refresh Request}}$ Inputs | $I_{IL}$ | – | – | -250 | μA |
| ($V_{CC}$ = 5.25 V, $V_{IL}$ = 0.5 V) | | | | | |
| $\overline{\text{Power-On Reset}}$ Input[1] | $I_{IL\overline{R}}$ | – | – | -250 | μA |
| ($V_{CC}$ = 5.25 V, $V_{IL}$ = 0.5 V) | | | | | |

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## OPERATING DYNAMIC POWER SUPPLY CURRENT

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power Supply Currents ($V_{CC}$ = 5.25 V, $f_{osc}$ = 8.0 MHz, $V_{IL}$ = 0 V, $V_{IH}$ = 3.0 V) | | | | | |
| Normal Operation (Memory Ready and $\overline{\text{DMA/Refresh Request}}$ Inputs at High Logic State) | $I_{CCN}$ | – | – | 150 | mA |
| Memory Ready Stretch Operation (Memory Ready Input at Low Logic State; $\overline{\text{DMA/Refresh Request}}$ Input at High Logic State) | $I_{CCMR}$ | – | – | 135 | mA |
| $\overline{\text{DMA/Refresh Request}}$ Stretch Operation (Memory Ready Input at High Logic State; $\overline{\text{DMA/Refresh Request}}$ Input at Low Logic State) | $I_{CCDR}$ | – | – | 135 | mA |

## SWITCHING CHARACTERISTICS

(These specifications apply whether the Internal Oscillator (see Figure 9) or an External Oscillator is used (see Figure 10). Typical values measured at $V_{CC}$ = 5.0 V, $T_A$ = 25°C, fo = 1.0 MHz (see Figure 8).

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **MPU $\phi$1 AND $\phi$2 CHARACTERISTICS** | | | | | |
| Output Period (Figure 3) | $t_o$ | 500 | – | – | ns |
| Pulse Width (Figure 3) | $t_{PWM}$ | | | | ns |
| (fo = 1.0 MHz) | | 400 | – | – | |
| (fo = 1.5 MHz) | | 230 | – | – | |
| (fo = 2.0 MHz) | | 180 | – | – | |
| Total Up Time (Figure 3) | $t_{UPM}$ | | | | ns |
| (fo = 1.0 MHz) | | 900 | – | – | |
| (fo = 1.5 MHz) | | 600 | – | – | |
| (fo = 2.0 MHz) | | 440 | – | – | |
| Delay Time Referenced to Output Complement (Figure 3) | | | | | |
| Output High to Low State (Clock Overlap at 1.0 V) | $t_{PLHM}$ | 0 | – | – | ns |
| Delay Times Referenced to 2 x fo (Figure 4 MPU $\phi$2 only) | | | | | |
| Output Low to High Logic State | $t_{PLHM2X}$ | – | – | 85 | ns |
| Output High to Low Logic State | $t_{PHLM2X}$ | – | – | 70 | ns |
| Transition Times (Figure 3) | | | | | |
| Output Low to High Logic State | $t_{TLHM}$ | – | – | 25 | ns |
| Output High to Low Logic State | $t_{THLM}$ | – | – | 25 | ns |
| **BUS $\phi$2 CHARACTERISTICS** | | | | | |
| Pulse Width – Low Logic State (Figure 4) | $t_{PWLB}$ | | | | ns |
| (fo = 1.0 MHz) | | 430 | – | – | |
| (fo = 1.5 MHz) | | 280 | – | – | |
| (fo = 2.0 MHz) | | 210 | – | – | |
| Pulse Width – High Logic State | $t_{PWHB}$ | | | | ns |
| (fo = 1.0 MHz) | | 450 | – | – | |
| (fo = 1.5 MHz) | | 295 | – | – | |
| (fo = 2.0 MHz) | | 235 | – | – | |
| Delay Times – (Referenced to MPU $\phi$1) (Figure 4) | | | | | |
| Output Low to High Logic State | $t_{PLHBM1}$ | | | | ns |
| (fo = 1.0 MHz) | | 480 | – | – | |
| (fo = 1.5 MHz) | | 320 | – | – | |
| (fo = 2.0 MHz) | | 240 | – | – | |
| Output High to Low Logic State | $t_{PHLBM1}$ | | | | |
| ($C_L$ = 300 pF) | | – | – | 25 | |
| ($C_L$ = 100 pF) | | – | – | 20 | |
| Delay Times (Referenced to MPU $\phi$2) (Figure 4) | | | | | |
| Output Low to High Logic State | $t_{PLHBM2}$ | -30 | – | +25 | ns |
| Output High to Low Logic State | $t_{PHLBM2}$ | 0 | – | +40 | ns |
| Transition Times (Figure 4) | | | | | |
| Output Low to High Logic State | $t_{TLHB}$ | – | – | 20 | ns |
| Output High to Low Logic State | $t_{THLB}$ | – | – | 20 | ns |

**SWITCHING CHARACTERISTICS (continued)**

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **MEMORY CLOCK CHARACTERISTICS** | | | | | |
| Delay Times (Referenced to MPU $\phi 2$) (Figure 4) | | | | | |
| Output Low to High Logic State | $t_{PLHCM}$ | -50 | – | +25 | ns |
| Output High to Low Logic State | $t_{PHLCM}$ | 0 | – | +40 | ns |
| Delay Times (Referenced to 2 x fo) (Figure 4) | | | | | |
| Output Low to High Logic State | $t_{PLHC2X}$ | – | – | 65 | ns |
| Output High to Low Logic State | $t_{PHLC2X}$ | – | – | 85 | ns |
| Transition Times (Figure 4) | | | | | |
| Output Low to High State | $t_{TLHC}$ | – | – | 25 | ns |
| Output High to Low State | $t_{THLC}$ | – | – | 25 | ns |
| **2 x fo CHARACTERISTICS** | | | | | |
| Delay Times (Referenced to 4 x fo) (Figure 4) | | | | | |
| Output Low to High Logic State | $t_{PLH2X}$ | – | – | 50 | ns |
| Output High to Low Logic State | $t_{PHL2X}$ | – | – | 65 | ns |
| Delay Time (Referenced to MPU $\phi 1$) (Figure 4) | | | | | |
| Output High to Low Logic State | $t_{PHL2XM1}$ | | | | ns |
| (fo = 1.0 MHz) | | 365 | – | – | |
| (fo = 1.5 MHz) | | 220 | – | – | |
| Transition Times (Figure 4) | | | | | |
| Output Low to High Logic State | $t_{TLH2X}$ | – | – | 25 | ns |
| Output High to Low Logic State | $t_{THL2X}$ | – | – | 25 | ns |
| **4 x fo CHARACTERISTICS** | | | | | |
| Delay Times (Referenced to Ext. In) (Figure 4) | | | | | |
| Output Low to High Logic State | $t_{PLH4X}$ | – | – | 50 | ns |
| Output High to Low Logic State | $t_{PHL4X}$ | – | – | 30 | ns |
| Transition Time (Figure 4) | | | | | |
| Output Low to High Logic State | $t_{TLH4X}$ | – | – | 25 | ns |
| Output High to Low Logic State | $t_{THL4X}$ | – | – | 25 | ns |
| **MEMORY READY CHARACTERISTICS** | | | | | |
| Set-Up Times (Figure 5) | | | | | |
| Low Input Logic State | $t_{SMRL}$ | 55 | – | – | ns |
| High Input Logic State | $t_{SMRH}$ | 75 | – | – | ns |
| Hold Time (Figure 5) | | | | | |
| Low Input Logic State | $t_{HMRL}$ | 10 | – | – | ns |
| **$\overline{\text{DMA}}$/REFRESH REQUEST CHARACTERISTICS** | | | | | |
| Set-Up Times (Figure 6) | | | | | |
| Low Input Logic State | $t_{SDRL}$ | 65 | – | – | ns |
| High Input Logic State | $t_{SDRH}$ | 75 | – | – | ns |
| Hold Time (Figure 6) | | | | | |
| Low Input Logic State | $t_{HDRL}$ | 10 | – | – | ns |
| **DMA/REFRESH GRANT CHARACTERISTICS** | | | | | |
| Delay Time Referenced to Memory Clock (Figure 6) | | | | | |
| Output Low to High Logic State | $t_{PLHG}$ | -15 | – | +25 | ns |
| Output High to Low Logic State | $t_{PHLG}$ | -25 | – | +15 | ns |
| Transition Times (Figure 6) | | | | | |
| Output Low to High Logic State | $t_{TLHG}$ | – | – | 25 | ns |
| Output High to Low Logic State | $t_{THLG}$ | – | – | 25 | ns |
| **$\overline{\text{RESET}}$ CHARACTERISTICS** | | | | | |
| Delay Time Referenced to Power-On Reset (Figure 7) | | | | | |
| Output Low to High Logic State | $t_{PLH\overline{R}}$ | – | – | 1000 | ns |
| Output High to Low Logic State | $t_{PHL\overline{R}}$ | – | – | 250 | ns |
| Transition Times (Figure 7) | | | | | |
| Output Low to High Logic State | $t_{TLH\overline{R}}$ | – | – | 100 | ns |
| Output High to Low Logic State | $t_{THL\overline{R}}$ | – | – | 50 | ns |

## DESCRIPTION OF PIN FUNCTIONS

- 4 x $f_o$ — A free running oscillator at four times the MPU clock rate useful for a system sync signal.
- 2 x $f_o$ — A free running oscillator at two times the MPU clock rate.
- $\overline{\text{DMA/REF REQ}}$ — An asynchronous input used to freeze the MPU clocks in the $\phi 1$ high, $\phi 2$ low state for dynamic memory refresh or cycle steal DMA (Direct Memory Access).
- REF GRANT — A synchronous output used to synchronize the refresh or DMA operation to the MPU.
- MEMORY READY — An asynchronous input used to freeze the MPU clocks in the $\phi 1$ low, $\phi 2$ high state for slow memory interface.
- MPU $\phi 1$ MPU $\phi 2$ — Capable of driving the $\phi 1$ and $\phi 2$ inputs on two MC6800s.
- BUS $\phi 2$ — An output nominally in phase with MPU $\phi 2$ having MC8T26A type drive capability.
- MEMORY CLOCK — An output nominally in phase with MPU $\phi 2$ which free runs during a refresh request cycle.
- $\overline{\text{POWER-ON RESET}}$ — A Schmitt trigger input which controls $\overline{\text{Reset}}$. A capacitor to ground is required to set the desired time constant. Internal 50 k resistor to $V_{CC}$. See General Design Suggestions for Manual Reset Operation.
- $\overline{\text{RESET}}$ — An output to the MPU and I/O devices.
- X1, X2 — Provision to attach a series resonant crystal or RC network.
- EXT IN — Allows driving by an external TTL signal to synchronous the MPU to an external system.

FIGURE 1 – BLOCK DIAGRAM

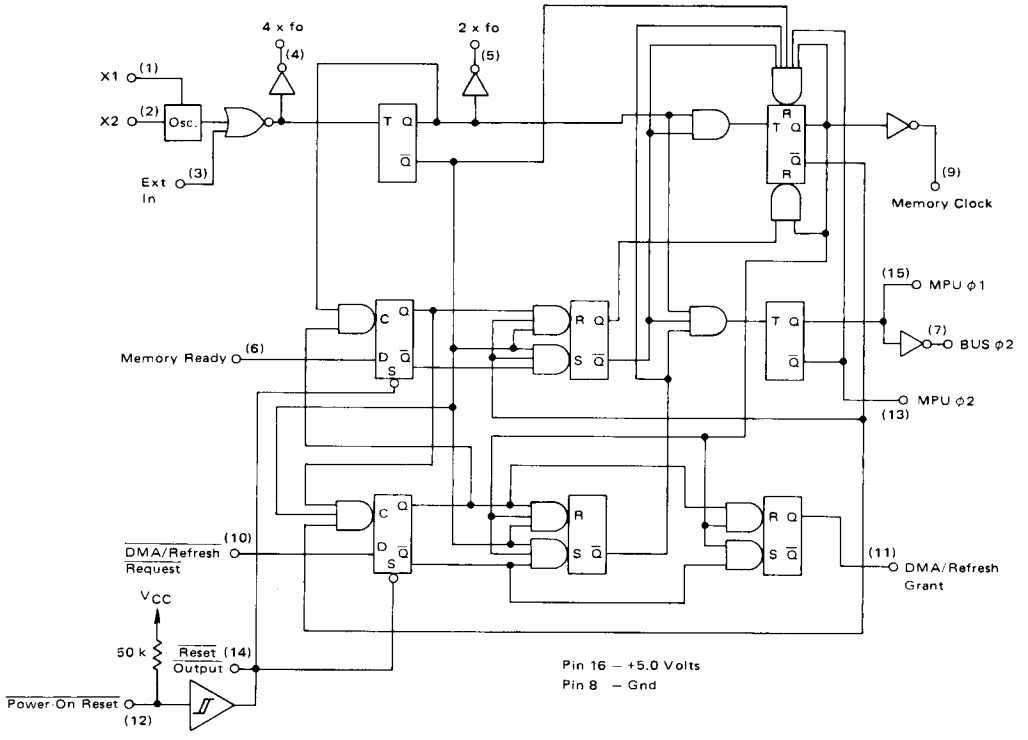



FIGURE 2 – TYPICAL HYSTERESIS CHARACTERISTIC OF RESET FUNCTION

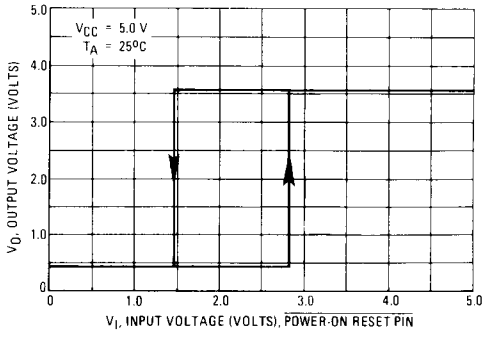
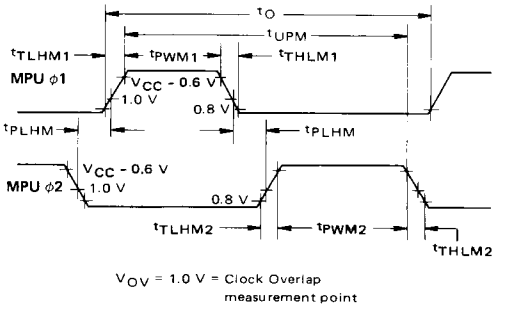



FIGURE 3 – TIMING DIAGRAM FOR MPU ϕ1 AND ϕ2




VOV = 1.0 V = Clock Overlap measurement point

FIGURE 4 – TIMING DIAGRAM FOR NON-STRETCHED OPERATION
(Memory Ready and $\overline{\text{DMA/Refresh Request}}$ held high continuously)
Ext. In Input Voltage: 0 V to 3.0 V, f = 8.0 MHz, Duty Cycle = 50%, $t_{TLHEX} = t_{THLEX} = 5.0$ ns

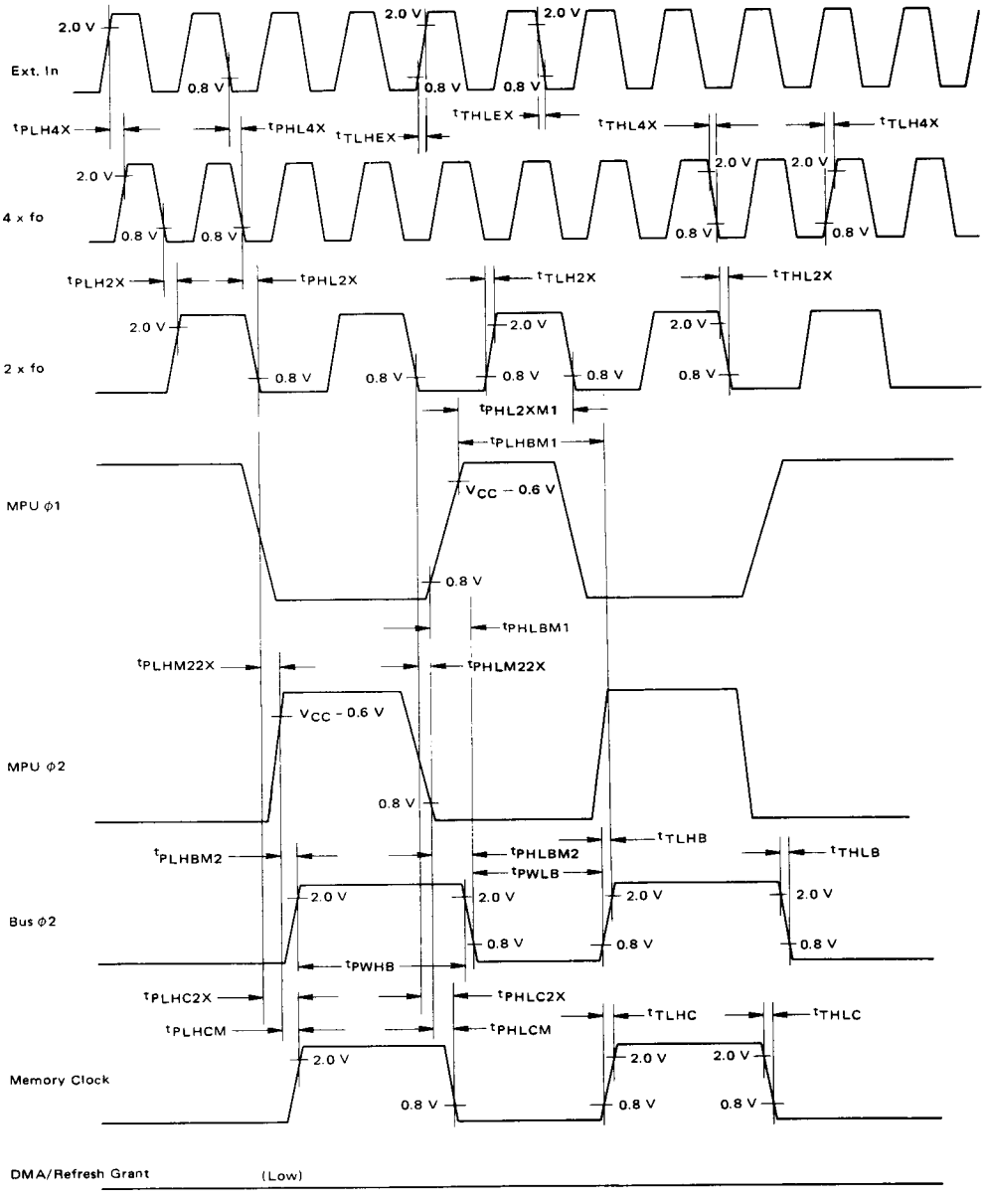



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FIGURE 5 – TIMING DIAGRAM FOR MEMORY READY STRETCH OPERATION
(Minimum Stretch Shown)
Input Voltage: 3.0 to 0 V, $t_{THLMR} = t_{TLHMR} = 5.0$ ns

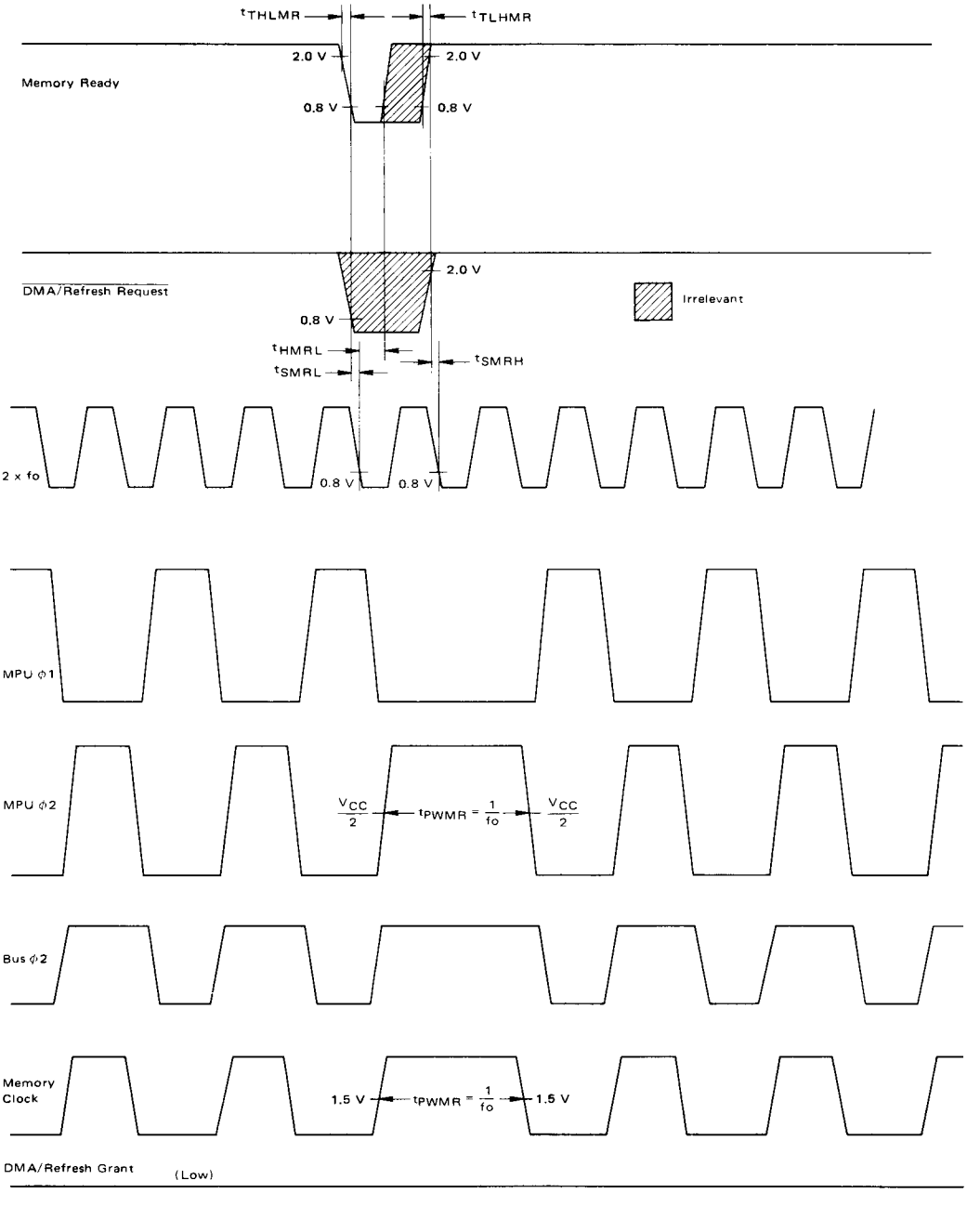

FIGURE 6 – TIMING DIAGRAM FOR $\overline{\text{DMA/REFRESH REQUEST}}$ STRETCH OPERATION
(Minimum Stretch Shown)
Input Voltage: 3.0 to 0 V, $t_{THLDR} = t_{TLHDR} = 5.0$ ns

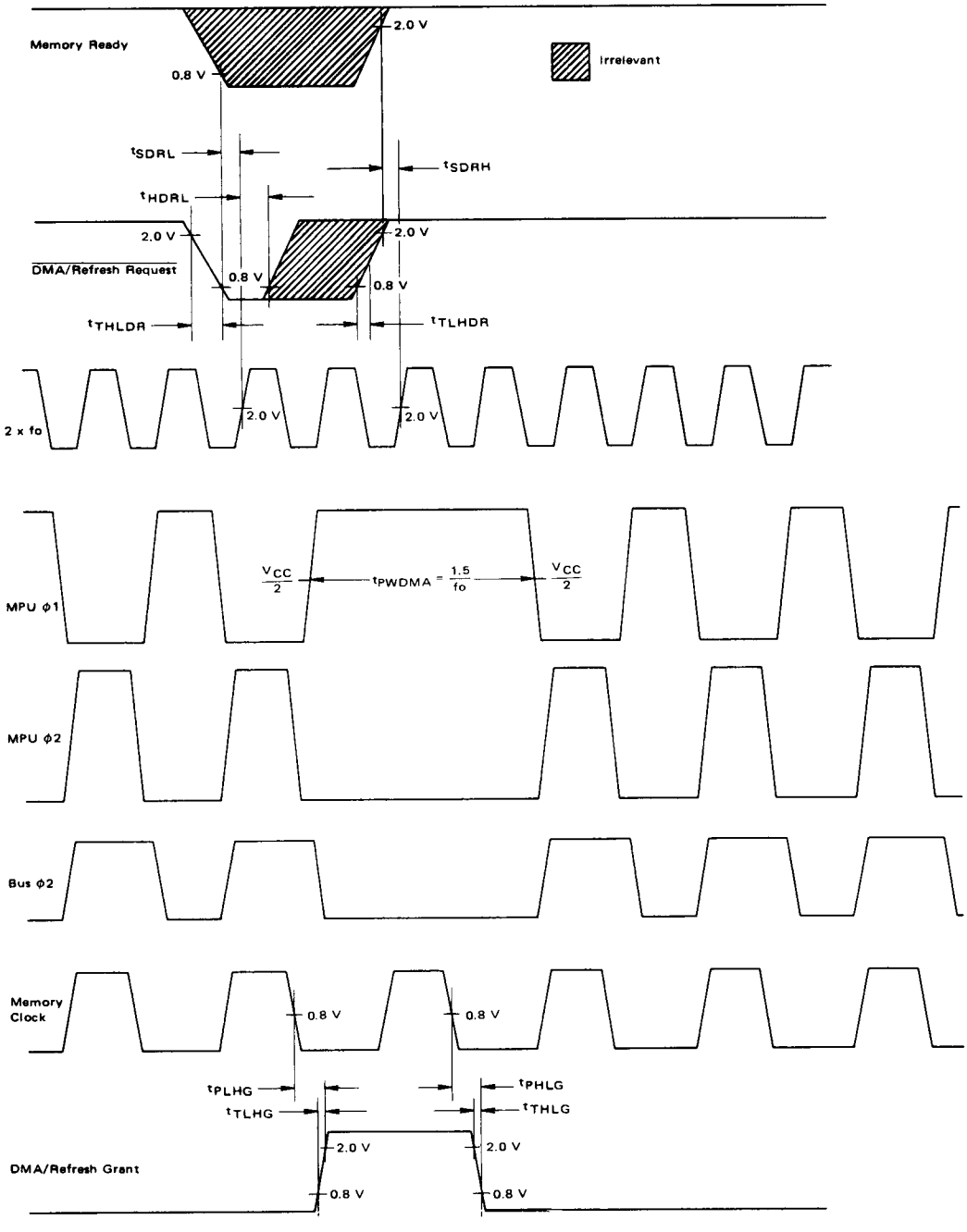


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FIGURE 7 – POWER ON RESET

Input Voltage: 0 to 5.0 V, f = 100 kHz – Pulse Width = 1.0 μs, $t_{TLH} = t_{THL}$ = 25 ns

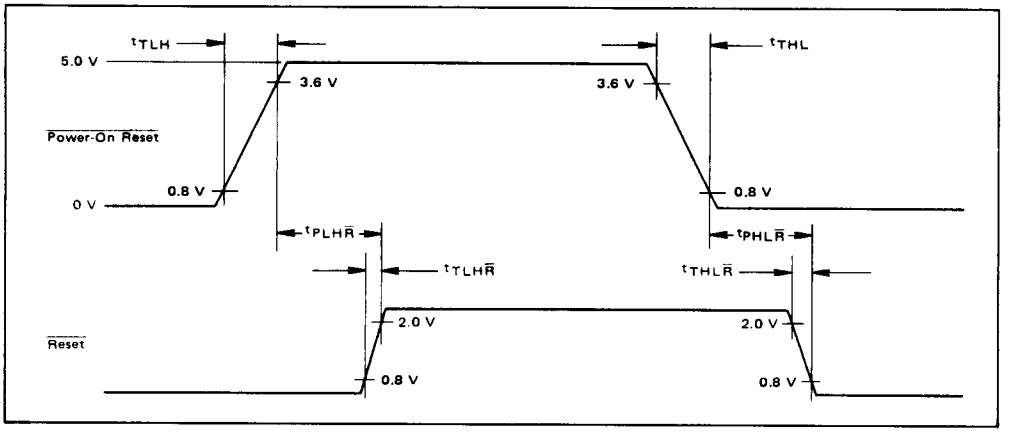
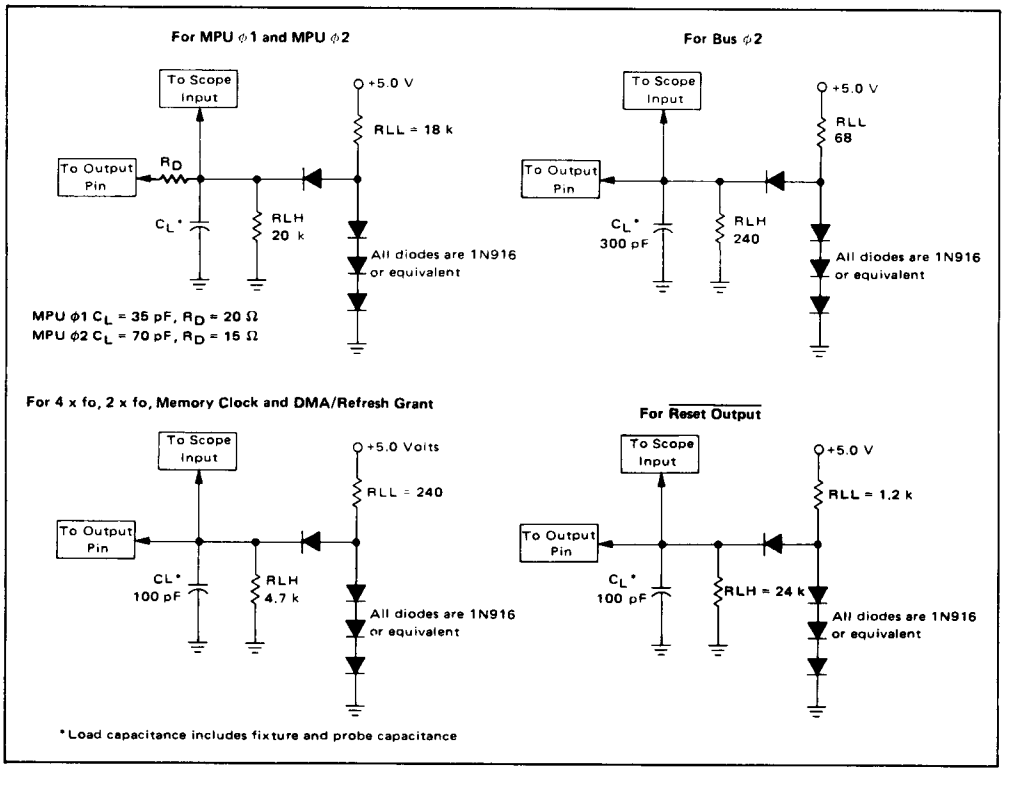



FIGURE 8 – LOAD CIRCUITS



## APPLICATIONS INFORMATION

FIGURE 9 – TYPICAL RC FREQUENCY versus VOLTAGE

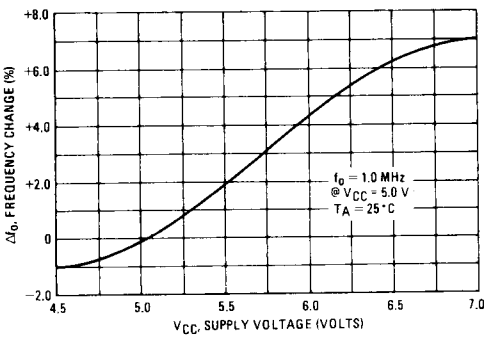



FIGURE 10 – TYPICAL RC FREQUENCY versus TEMPERATURE

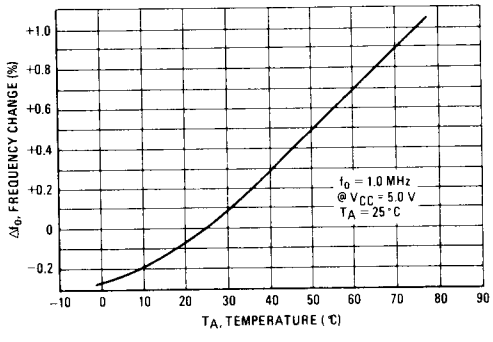
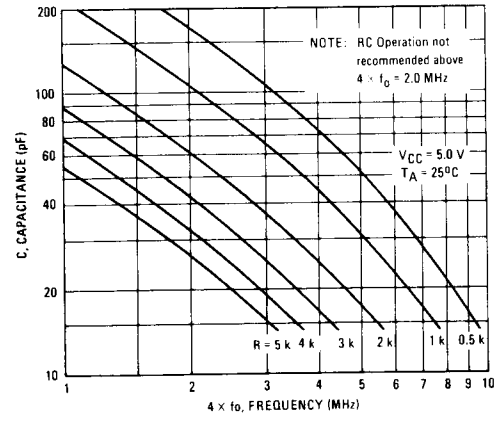



FIGURE 11 – TYPICAL FREQUENCY versus RESISTANCE FOR C VARIABLE




### GENERAL

The MC6875 Clock Generator/Driver should be located on the same board and within two inches of the MC6800 MPU. Series damping resistors of 10-30 ohms may be utilized between the MC6875 and the MC6800 on the $\phi 1$ and $\phi 2$ clocks to suppress overshoot and reflections.

The $V_{CC}$ pin (pin 16) of the MC6875 should be bypassed to the ground pin (pin 8) at the package with a 0.1 $\mu$F capacitor. Because of the high peak currents associated with driving highly capacitive loads, an adequately large ground strip to pin 8 should be used on the MC6875. Grounds should be carefully routed to minimize coupling of noise to the sensitive oscillator inputs. Unnecessary grounds or ground planes should be avoided near pin 2 or the frequency determining components. These components should be located as near as possible to the respective pins of the MC6875. Stray capacitance near pin 2 or the crystal, can affect the frequency. The can of the crystal should not be grounded. The ground side of the crystal or the C of the R-C oscillator should be connected as directly as possible to pin 8.

Unused inputs should be connected to $V_{CC}$ or ground. Memory Ready, $\overline{\text{DMA/Refresh Request}}$ and $\overline{\text{Power-On Reset}}$ should be connected to $V_{CC}$ when not used. The External Input should be connected to ground when not used.

### OSCILLATOR

A tank circuit tuned to the desired crystal frequency connected between terminals $X_1$ and $X_2$ as shown in Figure 12, is recommended to prevent the oscillator from starting at other than the desired frequency. The 1k$\Omega$ resistor reduces the Q sufficiently to maintain stable crystal control. Crystal manufacturers may recommend a capacitance ($C_L$) to be used in series with the crystal for optimum performance at series resonance.

See Figures 9 and 10 for typical oscillator temperature and $V_{CC}$ supply dependence for R-C operation.

FIGURE 12 – OSCILLATOR–CRYSTAL OPERATION

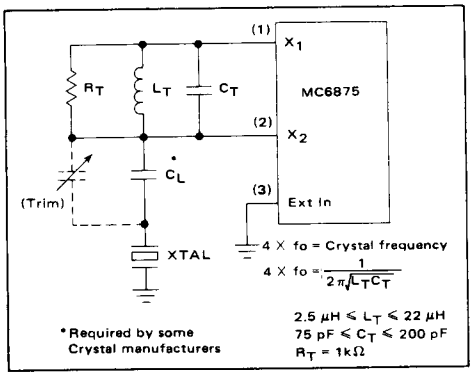
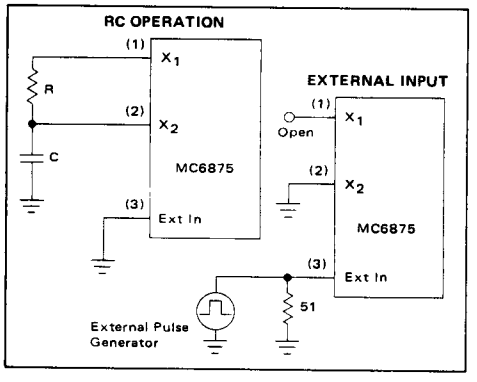


TABLE 1 – OSCILLATOR COMPONENTS

| TANK CIRCUIT PARAMETERS | | APPROXIMATE CRYSTAL PARAMETERS | | | | CTS KNIGHTS 400 REIMANN AVE. SANDWICH, IL 60548 (815) 786-8411 | McCOY ELECT. CO. WATTS & CHESTNUTS STS. MT. HOLLY SPRING, PA 17065 (717) 486-3411 | TYCO CRYSTAL PRODUCTS 3940 W. MONTECITO PHOENIX, AZ 85019 (602) 272-7945 |
|---|---|---|---|---|---|---|---|---|
| $L_T$ μH | $C_T$ pF | $R_S$ Ohms | $C_o$ pF | $C_1$ mpF | fo MHz | | | |
| 10 | 150 | 15-75 | 3-6 | 12 | 4.0 | MP-04A * 390 pF | 113-31 | 150-3260 |
| 4.7 | 82 | 8-45 | 4-7 | 23 | 8.0 | MP-080 * 47 pF | 113-32 | 150-3270 |

Inductors may be obtained from: Coilcraft, Cary, IL 60013 (312) 639-2361

FIGURE 13




7

To precisely time a crystal to desired frequency, a variable trimmer capacitor in the range of 7 to 40 pF would typically be used. Note it is not a recommended practice to tune the crystal with a parallel load capacitance.

The table above shows typical values for $C_T$ and $L_T$, typical crystal characteristics, and manufacturers' part numbers for 4.0 and 8.0 megahertz operation.

The MC6875 will function as an R-C oscillator when connected as shown in Figure 13. The desired output frequency (Mϕ1) is approximately:

Formula

$$4 \times fo \approx \frac{320}{C\,(R + .27) + 23}$$

C in picofarads
R in K ohms
4 x fo in Megahertz

(See Figure 11)

It would be desirable to select a capacitor greater than 15 pF to minimize the effects of stray capacitance. It is also desirable to keep the resistor in the 1 to 5 k Ω range. There is a nominal 270 Ω resistor internally at $X_1$ which is in series with the external R. By keeping the external R as large as possible, the effects due to process variations of the internal resistor on the frequency will be reduced. There will, however, still be some variation in frequency in a production lot both from the resistance variations, external and internal, and process variations of the input switching thresholds. Therefore, in a production system, it is recommended a potentiometer be placed in series with a fixed R between $X_1$ and $X_2$.

## POWER-ON RESET

As the power to the MC6875 comes up, the $\overline{\text{Reset Output}}$ will be in a high impedance state and will not give a solid $V_{OL}$ output level until $V_{CC}$ has reached 3.5 to 4.0 V. During this time transients may appear on the clock outputs as the oscillator begins to start. This happens at approximately $V_{CC}$ = 3 V. At some $V_{CC}$ level above that, where $\overline{\text{Reset Output}}$ goes low, all the clock outputs will begin functioning normally. This phenomenon of the start-up sequence should not cause any problems except possibly in systems with battery back-up memory. The transients on the clock lines during the time the $\overline{\text{Reset Output}}$ is high impedance could initiate the system in some unknown mode and possibly write into the backup memory system. Therefore in battery backup systems, more elaborate reset circuitry will be required.

Please note that the $\overline{\text{Power-On Reset}}$ input pin of the MC6875 is not suitable for use with a manual MPU reset switch if the $\overline{\text{DMA/Ref Req}}$ or Memory Ready inputs are going to be used. The power on reset circuitry is used to initialize the internal control logic and whenever the input is switched low, the MC6875 is irresponsive to the $\overline{\text{DMA/Ref Req}}$ or Memory Ready inputs. This may result in the loss of dynamic memory and/or possibly a byte of slow static memory. The circuit of Figure 14 is recommended for applications which do not utilize the $\overline{\text{DMA/Ref Req}}$ or Memory Ready inputs. The circuit of Figure 15 is recommended for those applications that do.

FIGURE 14 – MANUAL RESET FOR APPLICATIONS NOT USING $\overline{\text{DMA/REFRESH REQUEST}}$ OR MEMORY READY INPUTS

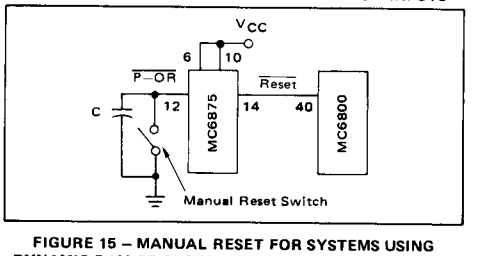



FIGURE 15 – MANUAL RESET FOR SYSTEMS USING DYNAMIC RAM OR SLOW STATIC RAM IN CONJUNCTION WITH MEMORY READY OR $\overline{\text{DMA/REFRESH REQUEST}}$ INPUTS