

PROGRAMMABLE INTERVAL TIMER

TMP82C53P-2

1. GENERAL DESCRIPTION

The TMP82C53P-2 (hereinafter referred to as TMP82C53) is a programmable counter/timer. It is organized as 3 independent 16 bit counters, each operates with a count rate of up to 5MHz. All modes of operation are software programmable.

2. FEATURES

- Count Binary or BCD
- 3 Independent 16 Bit Counters
- Single +5V Supply
- Count rate DC to 5MHz
- 6 programmable Counter Mode
- Low Power Consumption 5mA MAX. @5MHz
- Extended Operating Temperature -40°C to 85°C

3. PIN CONNECTIONS

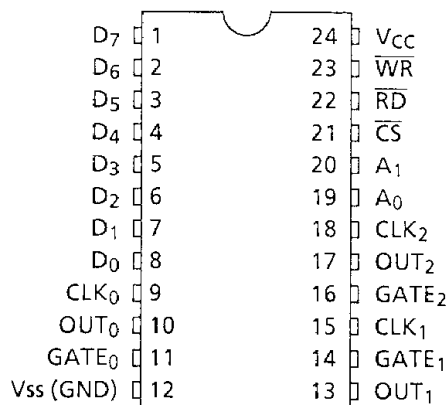


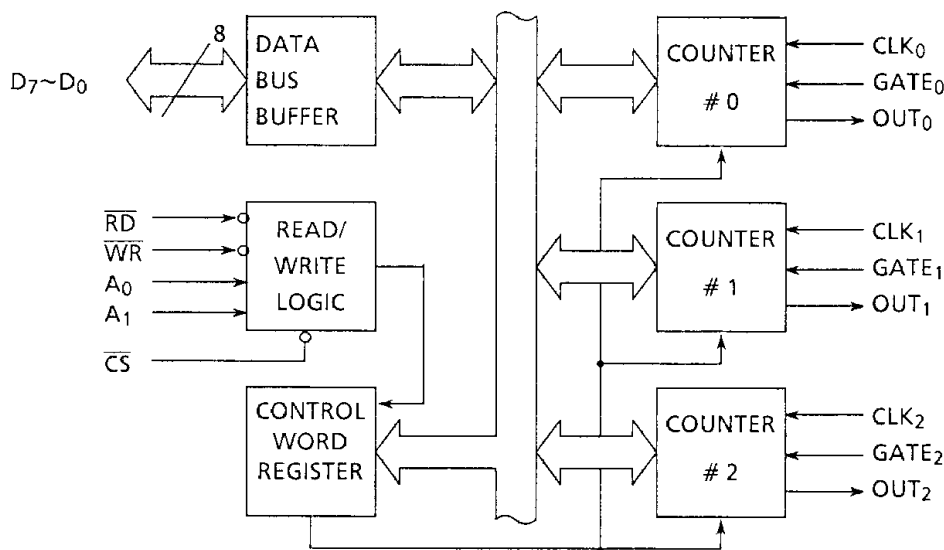
Table 3.1 PIN NAMES

D7~D0	Data Bus (8 bit)
CLK n	Counter Clock Input
GATE n	Counter Gate Input
OUT n	Counter Output
RD	Read Counter
WR	Write Counter
CS	Chip Select
A0~A1	Counter Select
Vcc	+5V
Vss	Ground(0v)

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4. BLOCK DIAGRAM



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5. PIN NAMES AND PIN DESCRIPTION

- V_{ss} (GND) (Power Supply)
Ground.
- V_{CC} (Power supply)
+5V during operation.
- \overline{CS} (Input)
A low level input on this pin enables read and write communication between the MPU and the TMP82C53. The \overline{CS} input has no effect upon the actual operation of the counters.
- A₀, A₁ (Input)
These inputs acts in conjunction with the \overline{CS} , \overline{WR} , and \overline{RD} pins. This pin is used to select one of the three counters to be operated on and to address the control word register for mode selection.
- \overline{WR} (Input)
A low level input on this pin when \overline{CS} is low enables the TMP82C53 to accept mode information or loading counters from the MPU.
- \overline{RD} (Input)
A low level input on this pin when \overline{CS} is low enables the TMP82C53 to output a counter value onto the data bus.

- D₀-D₇ (Input/Output)

Bidirectional 8bit data bus. Mode information and the count values are transferred via this data bus.
- CLK₀-CLK₂ (Input)

Clock inputs to counters. Falling edge on this pin enable the counter to count down.
- GATE₀-GATE₂ (Input)

Gate inputs to counters. The function of this pin differs by the mode selection of counter operation.
- OUT₀-OUT₂ (Output)

Outputs from the counters. The output signal from this pin differs by the mode selection of counter operation.

6. FUNCTIONAL DESCRIPTION

[Block Description]

Data Bus Buffer

This is 3-state, bidirectional, 8 bit buffer used for interfacing the TMP82C53 to the system data bus. The Data Bus Buffer has three functions as follows. Programming the MODEs of the TMP82C53, Loading the count registers, and Reading the count values.

Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and in turn generates control signals for overall device operation.

Table 6.1 Counter Addressing

\overline{CS}	\overline{RD}	\overline{WR}	A ₁	A ₀	
0	1	0	0	0	Load Counter #0
0	1	0	0	1	Load Counter #1
0	1	0	1	0	Load Counter #2
0	1	0	1	1	Write Mode Word
0	0	1	0	0	Read Counter #0
0	0	1	0	1	Read Counter #1
0	0	1	1	0	Read Counter #2
0	0	1	1	1	Data Bus is in High-impedance state
1	x	x	x	x	
0	1	1	x	x	

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Control Word Register

The Control Word Register is selected when A_0, A_1 are 11. It then accepts information from the data bus buffer and stores it in a register. The information stored in this register controls the operation mode of each counter, selection of binary or BCD counting and the loading of each count register. No reading of the contents of the control Word Register is available.

Counter #0, Counter #1, Counter #2

Since these three counters are identical, only a single counter will be described hereafter. Each counter consists of a single, 16bit, presettable, down counter. The counter can operate in either binary or BCD and its input, gate and output are configured by the selection of modes (6 modes: MODE 0 to MODE 5) stored in the Control Word Register. Also the control word handles the loading of the count value so that software overhead can be minimized for these functions.

The reading of the contents of each counter is available to the programmer with simple read operations for event counting applications. Special commands and logic are built in the TMP82C53 so that the contents of each counter can be read "on-the-fly" without having to inhibit the clock input.

[MODE Definition]

Mode 0: Interrupt on Terminal Count.

The output will be initially low after the mode set operation. After the count is loaded into the selected count register, the output will remain low and the counter will count. When terminal count is reached, the output will go high and remain high until the selected count register is reloaded with the mode or a new count value is loaded. The counter continues to decrement after terminal count has been reached.

Rewriting a counter register during counting results in the following:

- (1) Write 1st byte stops the current counting.
- (2) Write 2nd byte starts the new count.

MODE1: Programmable One Shot.

The output will go low on the count following the rising edge of the GATE input. The output will go high on the terminal count. If a new count value is loaded while the output is low it will not affect the duration of the one-shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse.

The one-shot is retriggerable, hence the output will remain low for the full count after any rising edge of the GATE input.

MODE2: Rate Generator

Divide by N counter. The output will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value. The GATE input, when low, will force the output high. When the GATE input goes high, the count will start from the initial count. Thus, the GATE input can be used to synchronize the counter.

When this mode is set, the output will remain high until after the count register is loaded. The output then can also be synchronized by software.

MODE 3: Square Wave Rate Generator

Similar to MODE 2 except that the output will remain high until one half the count has been completed (for even numbers) and go low for the other half of the count.

This is accomplished by decrementing the counter by two on the falling edge of each clock pulse. When the counter reaches terminal count, the state of the output is changed and the counter is reloaded with the full count and the whole process is repeated.

If the count is odd and the output is high, the first clock pulse (after the count is loaded) decrements the count by 1. Subsequent clock pulses decrement the count by 2. After timeout, the output goes low and the full count is reloaded. The first clock pulse (following the reload) decrements the counter by 3. Subsequent clock pulses decrement the count by 2 until timeout. Then the whole process is repeated. In this way, if the count is odd, the output will be high for $(N + 1)/2$ counts and low for $(N-1)/2$ counts.

MODE 4: Software Triggered Strobe

After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period, then will go high again.

If the count register is reloaded between output pulses, counting will continue from the new value. The count will be inhibited while the GATE input is low. Reloading the counter register will restart counting beginning with the new number.

MODE 5: Hardware Triggered Strobe

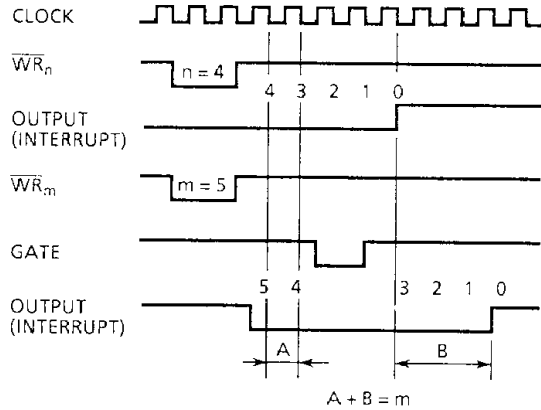
The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of any trigger.

Table 6.2 Gate Pin Operations

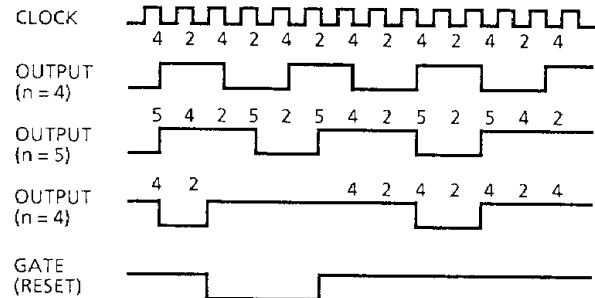
Status Modes	Low or Going Low	Rising	High
0	Disables counting	—	Enable counting
1	—	(1) Initiates counting (2) Resets output after next clock	
2	(1) Disables counting (2) Sets output immediately High	Initiates counting	Enable counting
3	(1) Disables counting (2) Sets output immediately High	Initiates counting	Enable counting
4	Disables counting	—	Enable counting
5	—	Initiates counting	—

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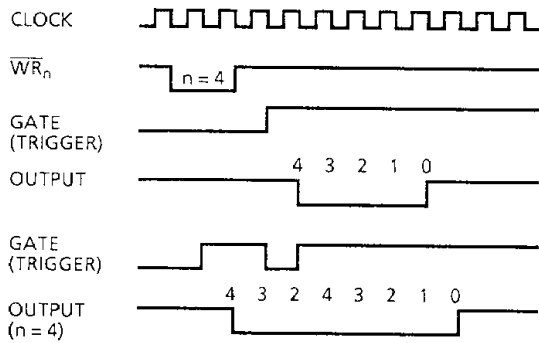
MODE0 : Interrupt on Terminal Count



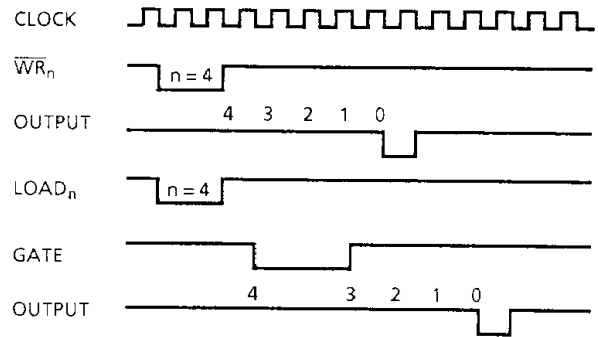
MODE3 : Square Wave Generator



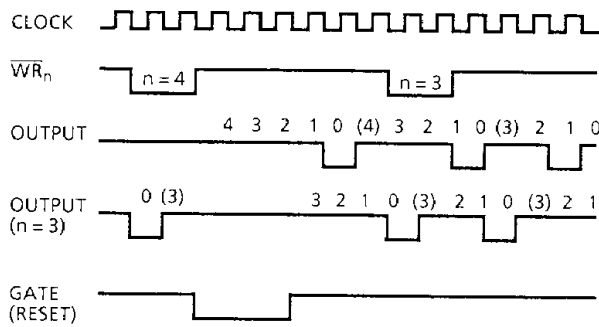
MODE1: Programmable One-Shot



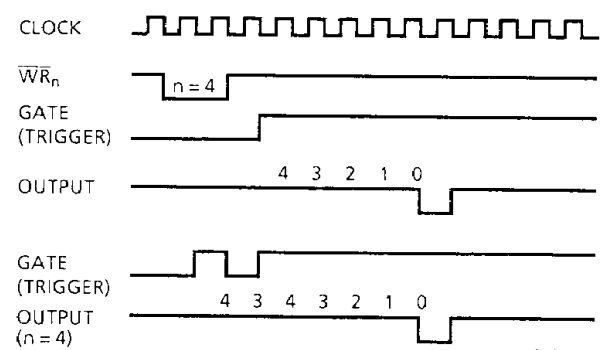
MODE4 : Software-Triggered Strobe



MODE2 : Rate Generator



MODE5 : Hardware-Triggered Strobe



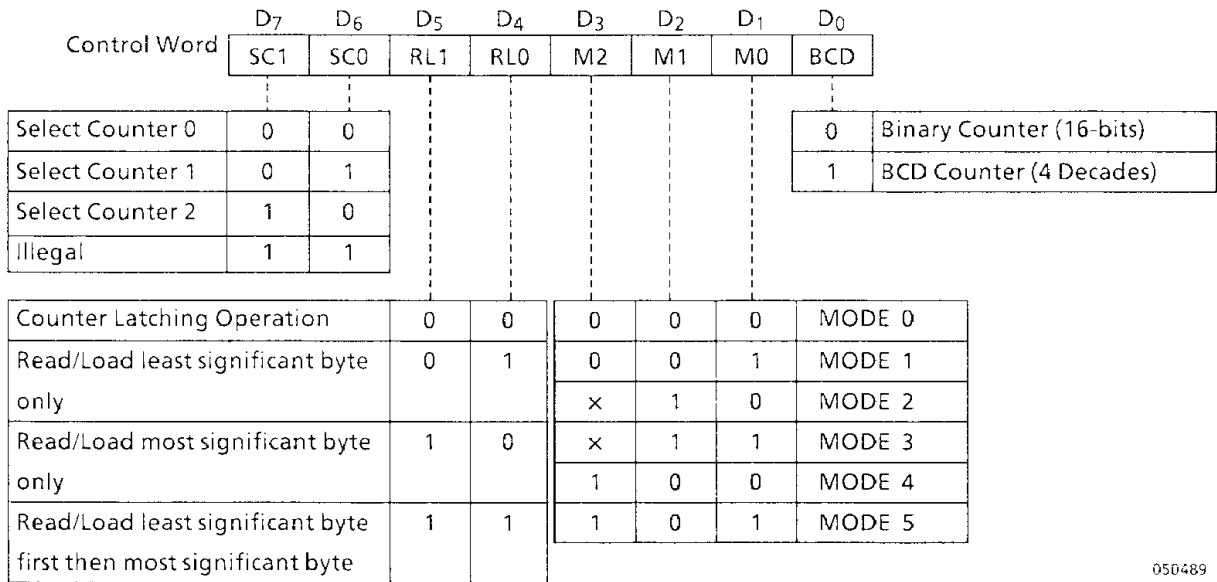
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Figure 6.1 TMP82C53 Timing Diagrams

7. PROGRAMMING THE TMP82C53

All of the MODEs for each counter are programmed by the systems software by simple I/O operations.

Each counter of the TMP82C53 is individually programmed by writing a control word into the Control Word Register. ($\overline{CS}=0, A_0=A_1=1, \overline{WR}=0$)



Note. SC: Select Counter, RL: Read/Load, M: Mode, BCD: Binary Coded Decimal.

The programmer must write out to the TMP82C53 a Mode Control Word and the programmed number of count register bytes (1 or 2) prior to actually using the selected counter.

The actual order of the programming is quite flexible. Writing out of the Mode Control Word can be in any sequence of counter selection.

The loading of the Count Register with actual count value, however, must be done in exactly the sequence programmed in the Mode Control Word (RL0, RL1).

8. Counter Loading

The count register is not loaded until the count value is written (one or two bytes, depending on the mode selected by the RL bits), followed by a rising edge and a falling edge of the clock.

The count register must be loaded with the number of bytes programmed in the Mode Control Word. The one or two bytes to be loaded in the count register do not have to follow the associated Mode Control Word. They can be programmed at any time following the Mode Control Word loading as long as the correct number of bytes is loaded in order.

All counters are down counters. Loading all zeros will result in the maximum count (2^{16} for Binary or 10^4 for BCD). In MODE 0 and MODE 4, the new count will not restart until the load has been completed.

9. Read Operations

The TMP82C53 contains the circuit that will allow the programmer to easily read the contents of any of the three counters without disturbing the actual count in progress.

There are two methods that the programmer can use to read the value of the counters. The first method involves the use of simple I/O read operations. By controlling the A_0 , A_1 inputs to the TMP82C53, the programmer can select the counter to be read. The only requirement with this method is that in order to assure a stable count reading the actual this method is that in order to assure a stable count reading the actual operation of the selected counter must be inhibited either by controlling the GATE input or by external logic that inhibits the clock input.

The contents of the counter selected must be read in the sequence programmed in the Mode Control Word (RL0, RL1). When RL0, RL1 is 11. First I/O Read contains the least significant byte (LSB), second I/O Read contains the most significant byte (MSB), and the two bytes must be read before any loading WR command can be sent to the same counter.

The second method allows the programmer to read the contents of any counter without effecting or disturbing the count operation. When the programmer wishes to read the contents of a selected counter "On-the-fly", a special code should be written to the Mode register so that the counter holds an accurate, stable count value. The programmer then issues a normal read command to the selected counter. The contents of the latched register must be read in the sequence programmed in the Mode Control Word (RL0, RL1). This commands has no effect on the counters mode.

10. Program Example

Set up sequence for counter #0	MVI	A, 00110000B	... #0, LSB-MSB, MODE 0, Binary
	OUT	CWAD	... The address of Control Word Register
	MVI	A, 53H	... LSB for counter #0
	OUT	CNT0	... The address of counter #0
	MVI	A, 82H	... MSB for counter #0
	OUT	CNT0	... The address of counter #0
	:		
	:		
READ the contents of counter #0	MVI	A, 0000XXXXB	
	OUT	CWAD	... Latching count
	IN	CNT0	... Read LSB of counter #0
	MOV	L, A	
	IN	CNT0	... Read MSB of counter #0
	MOV	H, A	
	:		
	:		
RELOAD to counter #0	MVI	A, 28H	
	OUT	CNT0	... Load LSB for counter #0
	MVI	A, 53H	
	OUT	CNT0	... Load MSB for counter #0

11. ELECTRIC CHARACTERISTICS

11.1 ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
VCC	Vcc Supply Voltage (with respect to Vss [GND])	- 0.5 to + 7.0	V
VIN	Input Voltage (with respect to Vss [GND])	- 0.5 to Vcc + 0.5	V
VOUT	Output Voltage (with respect to Vss [GND])	- 0.5 to Vcc + 0.5	V
PD	Power Dissipation	250	mW
Tsol	Soldering Temperature (Sodlring Time 10 sec)	260	°C
Tstg	Storage Temperature	- 65 to + 150	°C
Topr	Operating Temperature	- 40 to + 85	°C

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11.2 DC CHARACTERISTICS

Ta = - 40°C to + 85°C, Vcc = 5V ± 10%, Vss(GND) = 0V

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
VIL	Input Low Voltage		- 0.5		0.8	V
VIH	Input High Voltage		2.2		Vcc + 0.5	V
VOL	Output Low Voltage	IOL = 2.2mA			0.45	V
VOH1	Output High Voltage	IOH = - 400µA	2.4			V
VOH2	Output High Voltage	IOH = - 100µA	Vcc - 0.8			V
IIL	Inupt Leak Current	0V ≤ VIN ≤ Vcc			± 10	µA
IOFL	Output Leak Current	0.45V ≤ VOUL ≤ Vcc			± 10	µA
ICC1	Operating Supply Current	CLK = 5MHz VIH = Vcc - 0.2V VIL = 0.2V			5	mA
ICC2	Stand-by Supply Current	CLK = DC VIH = Vcc - 0.2V VIL = 0.2V			10	µA

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11.3 AC CHARACTERISTICS

$T_a = -40^{\circ}\text{C TO } +85^{\circ}\text{C}$, $V_{cc} = 5\text{V} \pm 10\%$, $V_{ss}(\text{GND}) = 0\text{V}$

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
tAR	Address Set-up Time ($\overline{\text{RD}}$)		30			ns
tRA	Address Hold Time ($\overline{\text{RD}}$)		0			ns
tRR	RD Pulse Width		180			ns
tRD	Valid Data ($\overline{\text{RD}}$)	CL = 150pF			140	ns
tDF	Data Floating ($\overline{\text{RD}}$)		10		85	ns
tRV	Recovery Time		250			ns
tAW	Address Set-up Time ($\overline{\text{WR}}$)		0			ns
tWA	Address Hold Time ($\overline{\text{WR}}$)		30			ns
tWW	$\overline{\text{WR}}$ Pulse Width		150			ns
tDW	Data Set-up time ($\overline{\text{WR}}$)		100			ns
tWD	Data Hold Time ($\overline{\text{WR}}$)		30			ns
tCLK	Clock Period		200		DC	ns
tPWH	CLK High Pulse Width		80			ns
tPWL	CLK Low Pulse Width		65			ns
tGW	GATE Width High		50			ns
tGL	GATE Width Low		50			ns
tGS	GATE Set-up Time (CLK)		70			ns
tGH	GATE Hold Time (CLK)		50			ns
tOD	Output Delay From (CLK)	CL = 150pF			200	ns
tODG	Output Delay From (GATE)	CL = 150pF			200	ns

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Note: AC timings measurements are referenced to $V_{IL} = 0.45\text{V}$, $V_{IH} = 2.4\text{V}$,
 $V_{OL} = 0.8\text{V}$, $V_{OH} = 2.2\text{V}$.

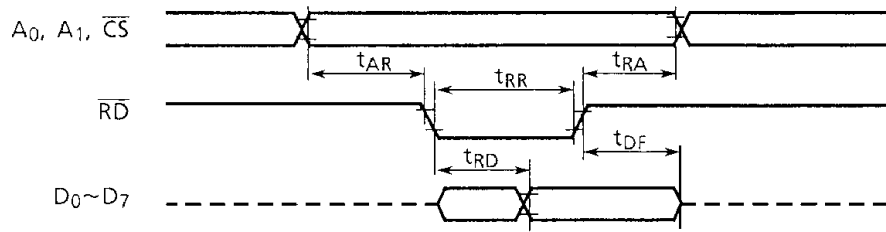
11.4 INPUT CAPACITANCE

$T_a = 25^{\circ}\text{C}$, $V_{cc} = V_{ss}(\text{GND}) = 0\text{V}$

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
CI	Input Capacitance	fC = 1MHz			10	pF
CI/O	Input/Output Capacitance	Unmeasured pins, 0V			20	

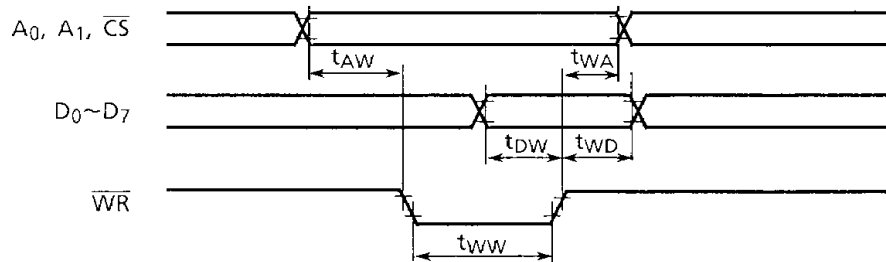
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12. TIMING DIAGRAM



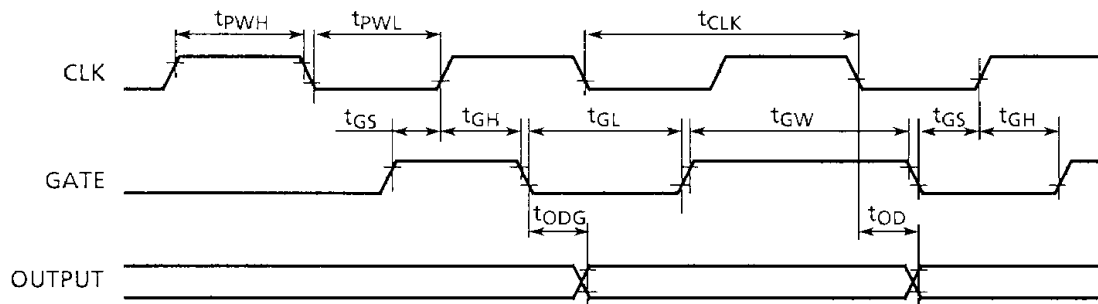
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Figure 12.1 Read Timing



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Figure 12.2 Write Timing



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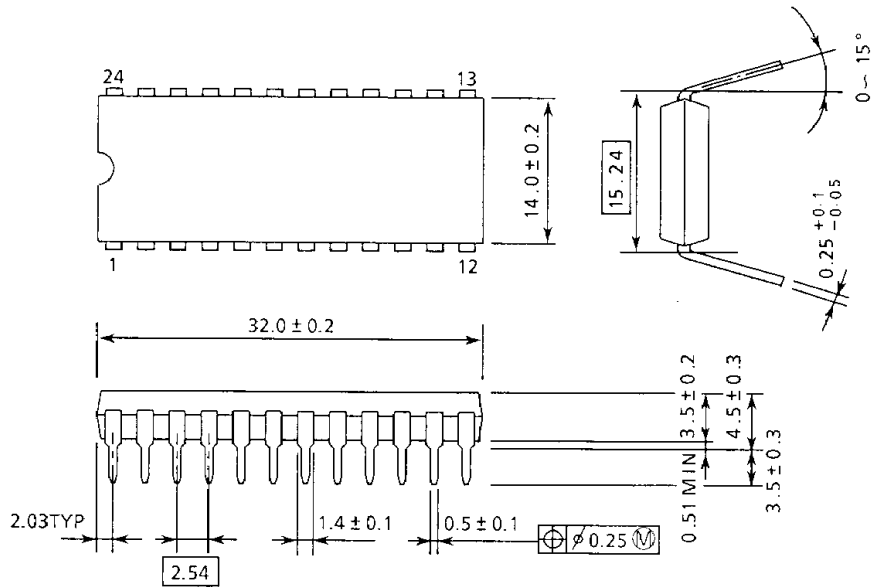
Figure 12.3 Clock & Gate Timing

13. EXTERNAL DIMENSION VIEW

13.1 24 Pin PLASTIC DIP

DIP24-P-600

Unit : mm



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Note : Lead pitch is 2.54mm and tolerance is ± 0.25 mm against theoretical center of each lead that is obtained on the basis of No.1 and No.24 leads.